Computer design

Speed, space and power estimation

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Building blocks

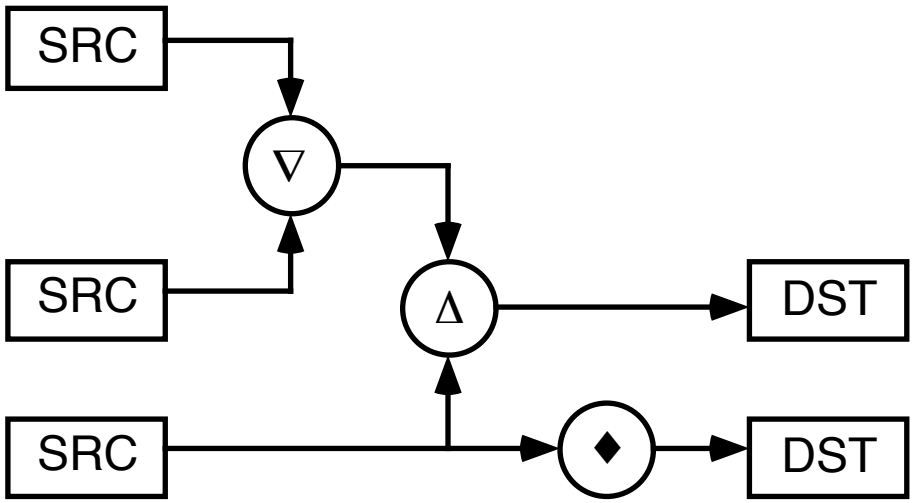
- See table in hand-out.
- Size
  - Given in "blocks"
  - Sizes may be scaled for different word widths, # of words
- Current and power
  - Given in mA and mW
  - May be scaled for different word width, # of words
- Delay
  - Given in nanoseconds (ns)
  - No load factor (fan-out effect)
  - Storage time is set-up plus hold time

Floor plans

- Arrangement and size of components on chip
- Keep distance small between communicating components
- Place external interfaces (lengthwise) at chip boundary
- Early floor planning is necessary to set space budgets
  - Intel i860 experience (example)
  - May determine size of cache, etc.
  - Can affect transistor sizing and performance
- Replication
  - Design one block and re-use it many times
  - Spread design cost over many instances of block
- Wiring
  - Routed (manually or automatically)
  - Abutment (adjacent placement of blocks)
- Regularity

Speed

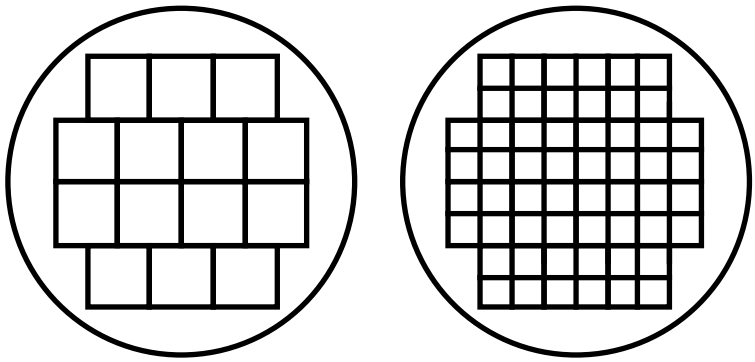
- Find minimum clock period
  - Find critical delay path through combinational logic
    - Simply add delays along paths
    - Square root of the sum of the squares
  - Add in set-up and hold time
  - Latches may also have a minimum pulse width
- Delay times can be affected by fan-out
  - Estimate wire capacitance
    - Measure wire width and length
    - Width × length × capacitance per unit area
  - Estimate gate load
    - Count number of (transistor) gates driven
    - Number of gates × capacitance per gate



- Path A: ∇ *delay* + Δ *delay* + *set-up* + *hold*

Space

- Decrease space to get more chips per wafer
- Wafer processing cost is fixed
- Spread cost of production over more units



$10,000 / 14 $10,000 / 56

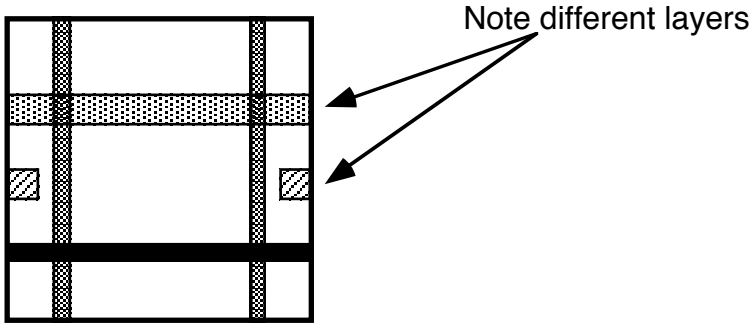
- Yield
  - Percentage of working chips (no defects)
  - Assume defects are random distributed
    - Poisson distribution
    - N fatal flaws per unit area
    - Let A be chip area
    - Probability of a good chip (zero defects)

$$P_0(NA) = e^{-NA}$$

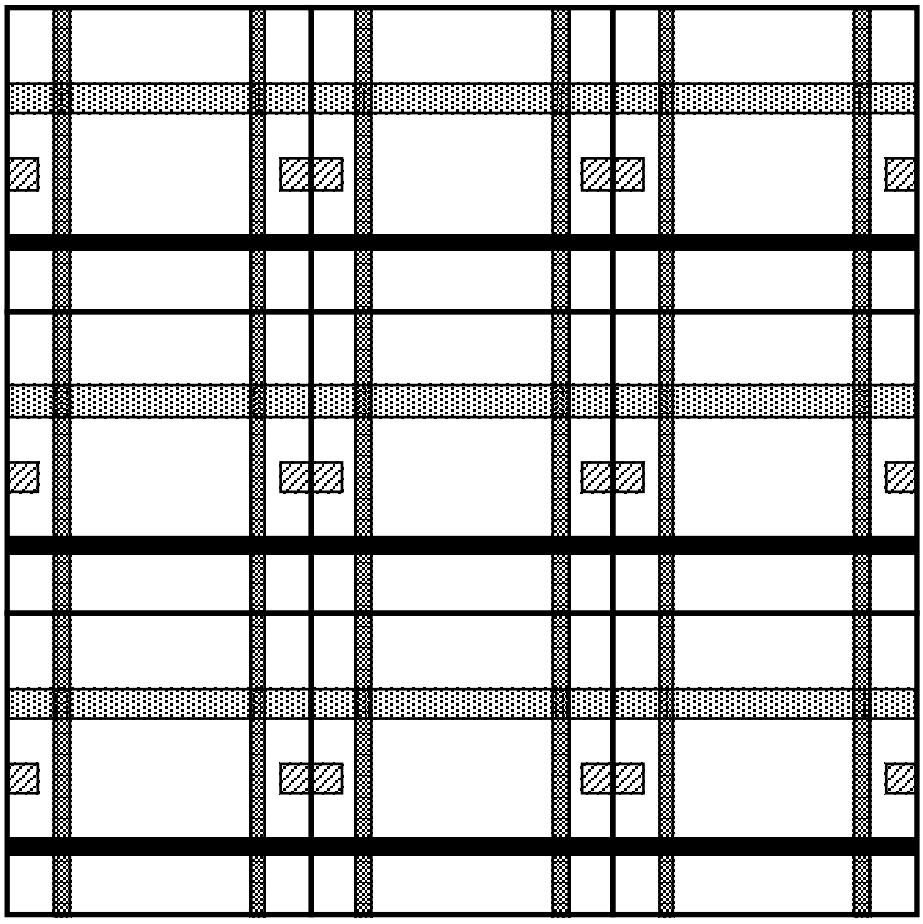
  - Keep area small (near $1 / N$)
- Space estimation (floor planning)
  - Active area = Σ component areas
  - % active area = Active area / total area
  - % wire area = 1 - % active area
  - Some chips may require 80% wire area!

Regularity and wiring

- Single cell with wiring



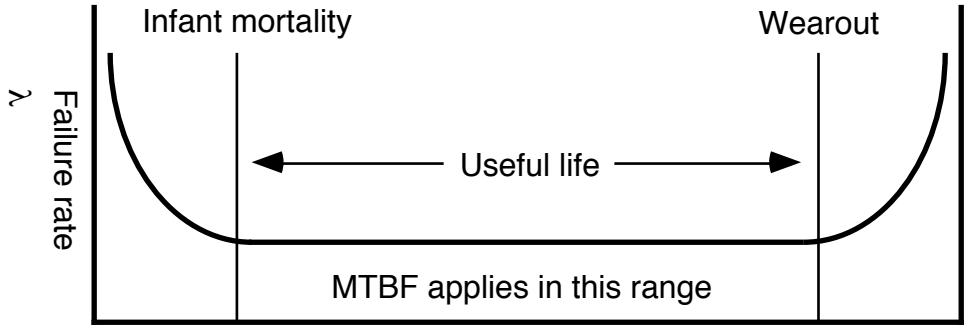
- Three by three array



Current and power

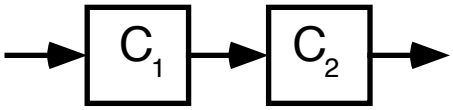
- Current estimation
  - Power grid sizing (maximum current density)
  - Total current = Σ component current requirements
- Power estimation
  - Maximum chip operating temperature (ambient)
  - High temperature increases stress
  - High stress accelerates aging
  - Stress reduces reliability
  - Thermal limits of packaging and cooling scheme
    - Air cooling: 0.05 Watts per cm^2 of board area
    - 20 cm^2 of board area per 1 cm^2 chip area
    - Chip dissipation should be about 1 Watt
    - 2 - 5 Watts is easily accomodated with air cooling
  - Total power = Σ component dissipation

Bathtub curve



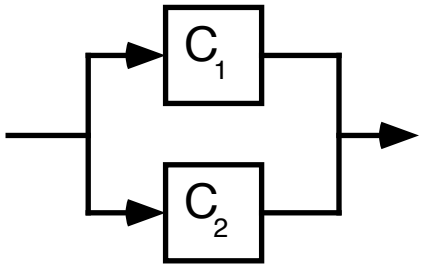
- Composition of three curves
- Early failure: Rate decreases with time
- Useful life: Random failure (exponential)
- Wearout: Rate increases with time

Components in series



- $R(t) = R_1(t) \times R_2(t)$
- $R(t) \leq \min[R_1(t), R_2$

Components in parallel



- $R(t) = 1 - [1 - R_1(t)] \times \ldots \times [1 - R_n$

Reliability

The reliability of a component at time t is defined as $R(t) = P(T > t)$, where T is the life time of the component. R is called the "reliability function."

Reliability equals the probability that the component is still functioning at time t.

Normal failure model

- Normal distribution
- Most items fail around the mean failure time
- 95.72 percent of failures occur $\pm 2\sigma$
- High reliability $\Rightarrow$ operating time much less than mean

Exponential failure law

- Exponential distribution
- Failure rate is constant
- No "wearing out" or aging effect
- Probability of failure is independent of past history
- Failure may be due to transient external event
- Event occurence constitutes a Poisson process.

Weibull failure law

- Weibull distribution
- Exponential distribution is a special case
- Failure due to "most severe flaw" of many flaws

MTBF

- Mean time between failure (MTBF.)
- Measurement
  - MTBF = Operating hours / Number of failures
  - Implies a constant failure rate
- Prediction
  - Information required
    - Component failure rates (at temperature)
    - Structure model (series, parallel)
    - Duty cycle
  - Typical system
    - Constant failure rate
    - Series non-redundant design
    - System fails if any one component fails
    - MTBF is reciprocal of sum of individual failure rates
    - MTBF = $1 / \Sigma \lambda$

- Example
  - Failure rates: 4.5×10^{-6}, 2.0×10^{-6}, 7.5×10^{-6}
  - MTBF = $1 / (4.5 + 2.0 + 7.5) \times 10^{-6} = 71{,}429$

- Duty cycle
  - Device may have different operating modes
  - Modes may have different failure rates
  - Example: Disk drive can be busy or idle
  - MTBF = $1 / DC_b (\lambda_b) + DC_i (\lambda_i)$