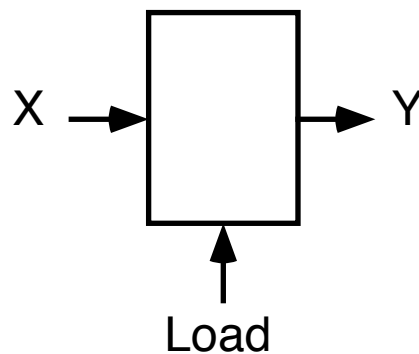# Computer design

System building blocks
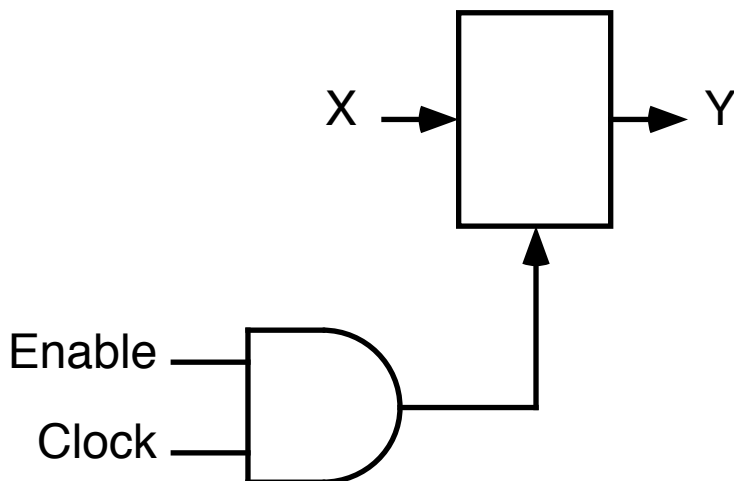
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Simple register

- Simple register
- Intrinsic operations
    - Load - write a new value into the register
    - Clear - set the register value to zero
- No "read" operation is necessary
- Current register value is always available at output

X → [ ] → Y

Load

- Number of bits set by replication across word length
- Common modes of operation
    - D-type latch (output follows input when clock asserted)
    - Master-slave (two-phase operation)

X → [ ] → Y

Enable ──┐
         ├─)──
Clock ───┘

Registers

- Counting register (counter)
    - Instruction pointer, stack pointer, loop counter
    - Intrinsic operations
        - Load - write a new value into the register
        - Clear - set the register value to zero
        - Up - increment value by one
        - Down - decrement value by one

- Shift register
    - Arithmetic accumulator, multiply
    - Intrinsic operations
        - Load - store new value
        - Clear - store zero in register
        - Left - logical/arithmetic shift or rotate left
        - Right - logical/arithmetic shift or rotate right

- Register file
    - General register set, stack
    - Intrinsic operations
        - Read - read value at address
   - Write - store value at address
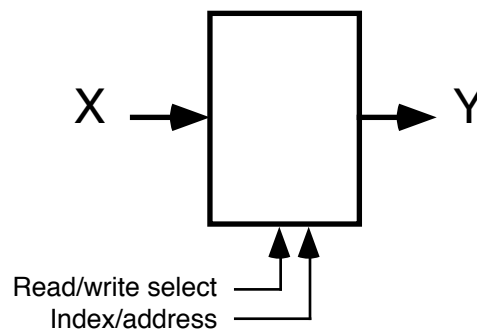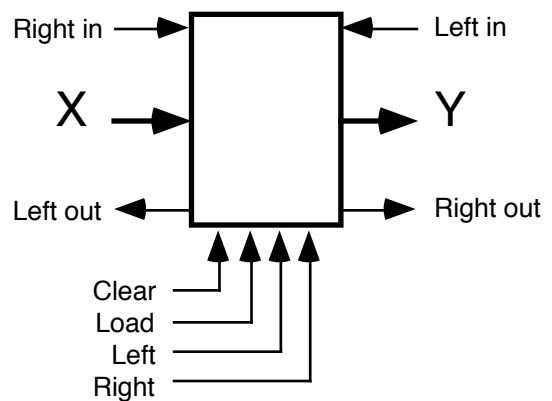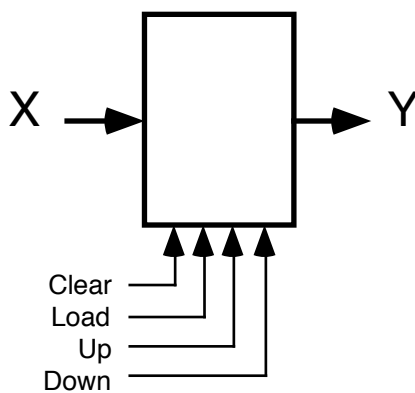
General registers

- Register to register architecture
  R [i] ← R [j] Δ R [k]
- Single port RAM implementation
  - Only one value can be read at a time
  - Sequential computation needed
    X ← R [j]
    Y ← Y Δ R [k]
    R [i] ← Y
- Dual port RAM implementation
  - Two read ports; two values out at a time
  - Reduce to two step evaluation
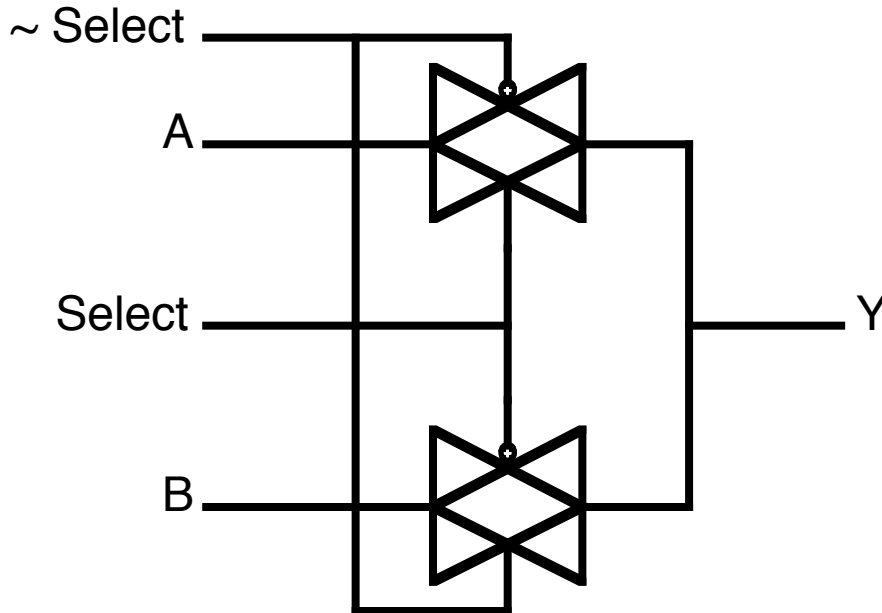   Y ← R [j] Δ R [k]
    R [i] ← Y
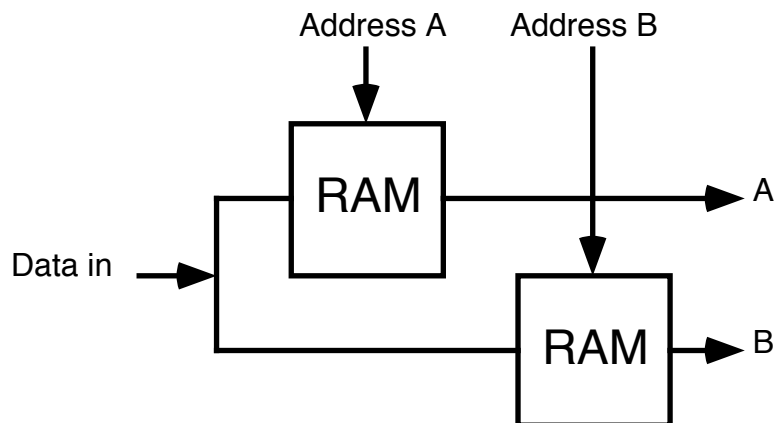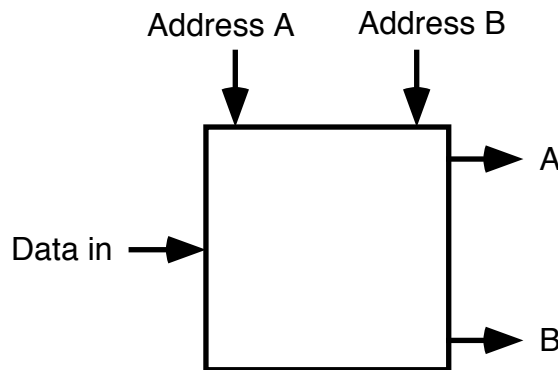
Multiplexer (selection)

- Select one of many inputs
- Standard multiplexer design
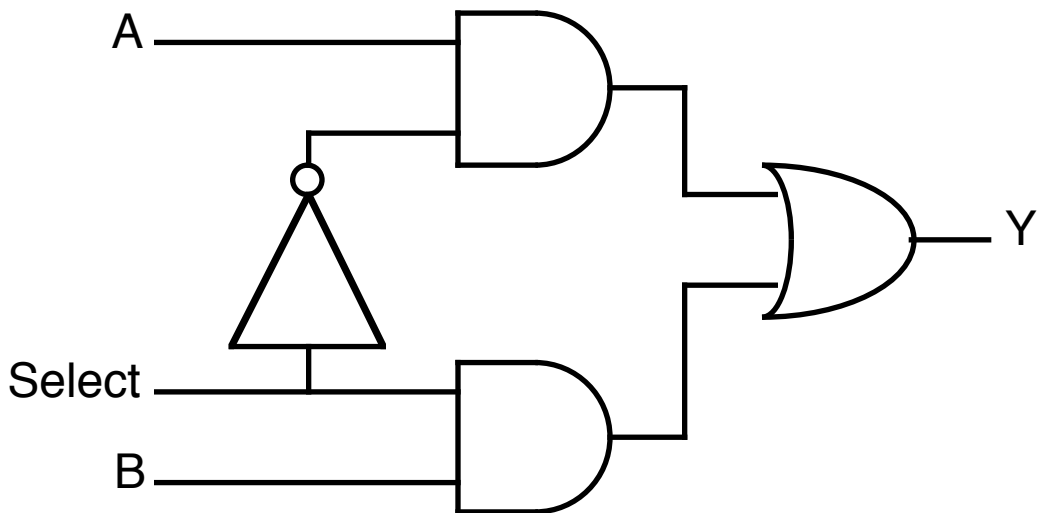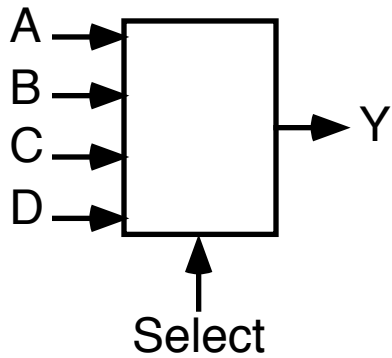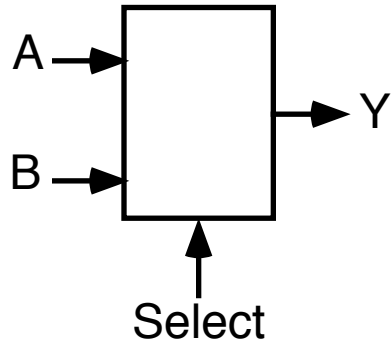
Selection

- Technology dependent features can be exploited
- CMOS mux uses two 2-transistor transmission gates
- Small size (versus 12 transistors)
- Simpler Vdd and ground wire routing
- Lower current consumption and power dissipation

- Tri-state shared bus
- Three states
  - Two logic states (0 and 1)
  - High impedence state (Z)
  - Electrically connects and disconnects to common bus
  - Selection function is distributed to senders
  - No central multiplexer; wiring is simpler
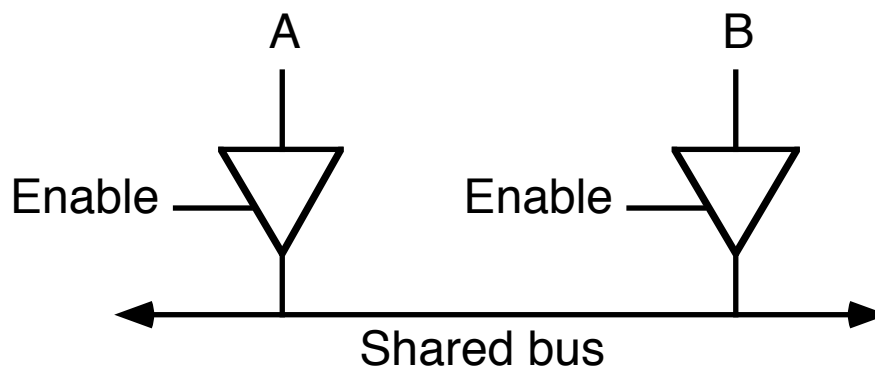
Decoders

- Input N-digit unsigned binary value
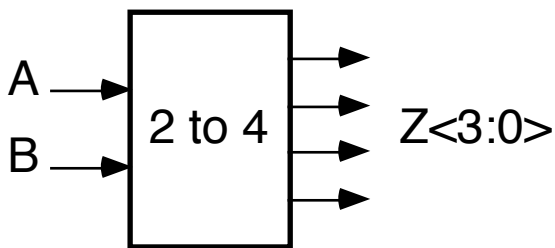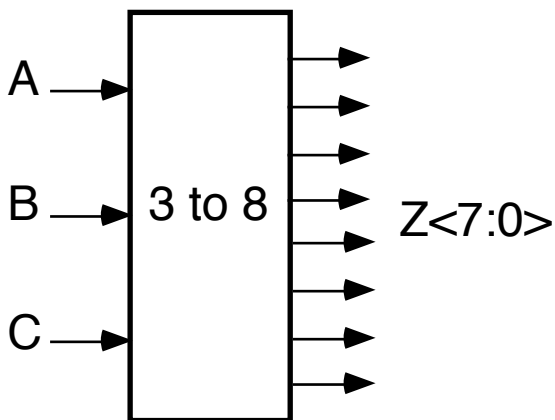- Assert one of 2^N output lines
- May be driven low- or high-true
- Used for address and control line decoding

A →
B → [2 to 4] → Z<3:0>

A	B	Z0	Z1	Z2	Z3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

A →
B → [3 to 8] → Z<7:0>
C →

| A	B	C	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Low-true decoder

Programmable structures

- Programmable logic array (PLA)
  - Implements sum of products logic equation
  - "AND" plane to form product terms
  - "OR" plane to form sum of products
  - Planes are programmed to make connection to inputs
  - Logic is easy to change; regular layout
  - Good for finite state machines
  - Not minimum space or power implementation
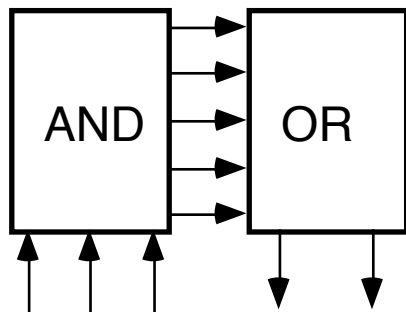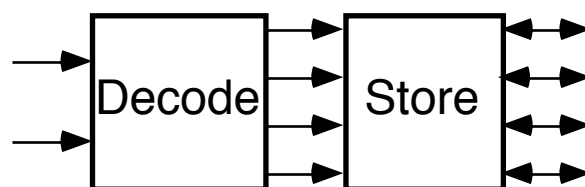
```
  AND  →  OR
```
  - Three inputs
  - Two output
  - Five product terms
  - True and complement of inputs

- Read only memory
  - Address decoder (fully decoded AND plane)
  - High density plane of unalterable data bits
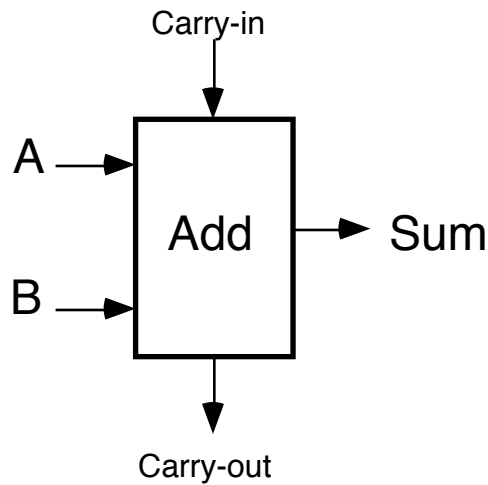
```
  Decode  →  Store  →
```
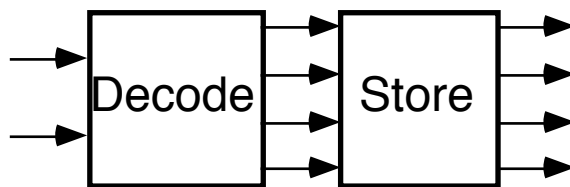
- Random access, read-write memory
  - Static - nonvolatile, higher power
  - Dynamic - charge leakage, data must be refreshed

```
  Decode  →  Store  ↔
```
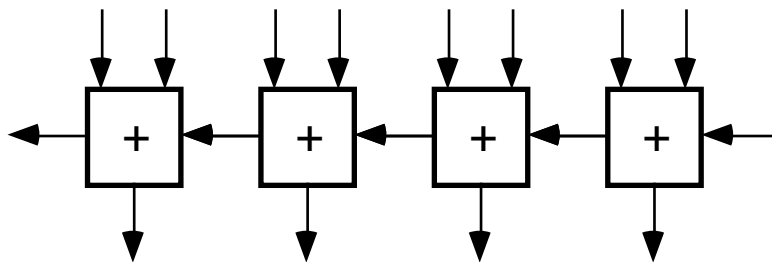 - Bi-directional data bus
  - Separate data in / out

Addition

Carry-in

A → Add → Sum

B →

Carry-out
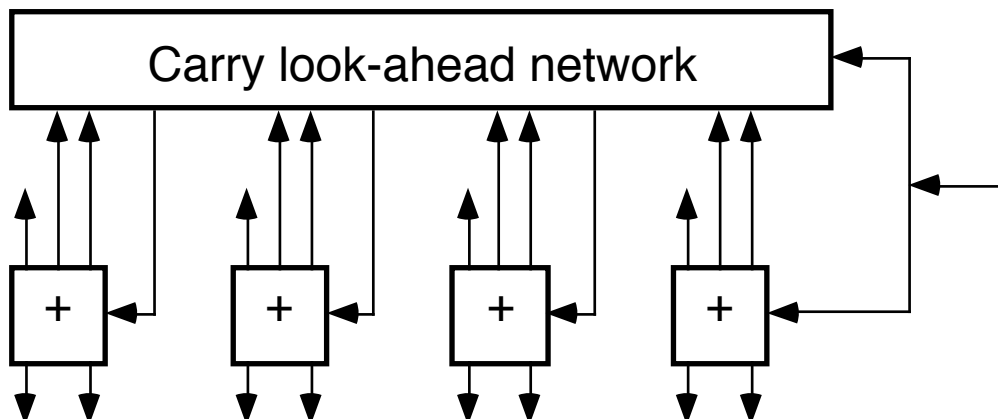
- Replicate full adder elements to desired word length
- Ripple carry adder
- Each adder forms sum and carry-out
- Carries must propagate through all stages - slow
- Sum = A ⊗ B ⊗ Cin, Cout = (A∧B) ∨ (A∧Cin) ∨

+ + + +

- Carry lookahead - generate and propagate carry-ins
- G = A ∧ B, P = A ⊗ B

Carry look-ahead network

+ + + +

Arithmetic logic unit (ALU)

- Common arithmetic operations
    - Two's complement representation
    - Add, subtract, incr/decrement, left shift (add to self)
    - Two's complement (negate and add one)
    - *Not* multiply or divide
- Common logic operations
    - One's complement (NOT)
    - Bit-wise AND, OR, exclusive-OR
- Processor conditions
    - Negative (sign bit of result)
    - Zero result
    - Overflow (undesired change in sign bit)

Carry-out

A → Result

B → Conditions (N, Z, V)

Carry-in
Operation

Comparator

A → A <

A =

B → A >
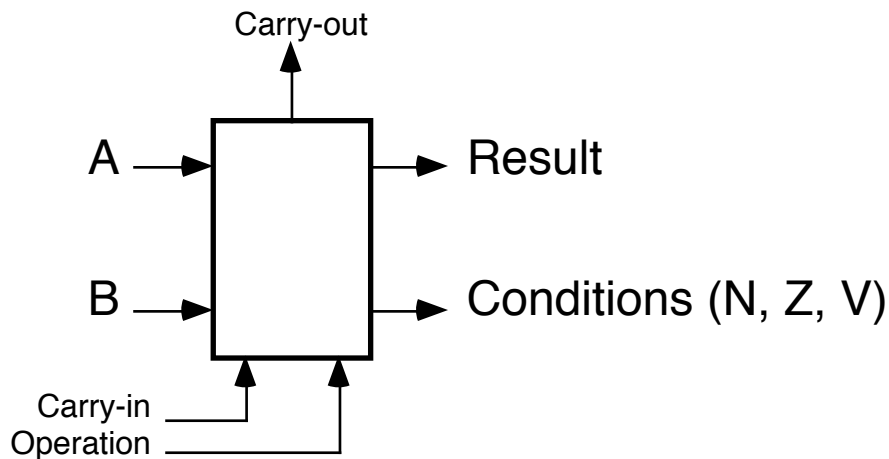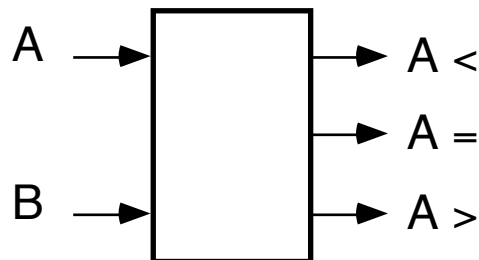
External input / output

- Chip must be connected to printed circuit board
    - Die is mounted in a carrier package
    - Carrier has traces leading to pins
    - Pins connect to PCB-level pads and wires
    - Wires must be bonded to chip and carrier traces
    - Chip connections are made to metal "bonding pads"
    - Pads must be placed at perimeter of die
- Typical component sizes (1 μm = 1 micron)
    - Transistor: 1 μm $\times$ 1 μm
    - Metal wire: 3 μm wide
    - Bonding pad: 100 μm $\times$ 100 μm
    - Human hair: 40 μm diameter
- Input
    - Voltage level shifting or hysteresis
    - Static protection
- Output
    - Must drive large off-chip wires (10+ pF capacitance)
    - Drive transistor: 80 μm $\times$ 1 μm
    - Large current requirement and power dissipation
- Bidirectional
    - Permits bidirectional flow of data
    - Must have a disconnected (high-Z) state
- Power supply (e.g., Vdd and ground)