Computer and VLSI design

Technology

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System design considerations

- Schedule
  - Time is money
  - Shorten development time and costs
  - Decrease time to market
  - Increase productivity through CAD tools
- Mechanical design
  - Pin, package, board, backplane, cabinet
  - Increase functionality per unit space
- Cooling
  - Convection, forced air, liquid cooling
  - Maximize function performed for heat dissipated
- Interconnection
  - PCB and backplane wiring capacitances are high
  - Decrease wire length and capacitance
- Reliability
  - Mechanical connections are least reliable
  - Decrease component and connection count
- Maintenance
  - Maximize availability
  - Fault detection and isolation
  - Maintenance strategy
    - Replace failed component or module
    - Repair failed module on-site

VLSI technology

- Mechanical
  - More functionality per package
  - Fewer packages, smaller and fewer boards, etc.
- Interconnection
  - Less board level interconnect
  - Lower wire capacitance ⇒ higher speed
  - Interconnect routing problem is moved to chip design
- Power supply
  - Lower (on-chip) wire capacitance
  - Less power to charge and discharge wires
- Cooling
  - Lower power may reduce system level costs
  - High circuit density may require special cooling
  - CMOS, for example, runs hotter at higher clock rate
- Maintenance
  - Chip replacement strategy is feasible
  - Fewer part types ⇒ smaller parts inventory
- Other opportunities
  - Volume production is (relatively) inexpensive
  - Combine processors and memory in vast quantities
  - Logic enhanced memories
  - Redundant components can be designed in

Full custom design

- Considerations
  - Knowledge of physical electronics
  - Process technology
  - Device sizing
  - Structural and physical partitioning
  - Floor plan
  - Interconnect routing
- Tools
  - Electrical simulation (SPICE)
  - Switch level simulation
  - Geometry (layout) editor
  - Silicon compiler
  - Net-list extraction

Semi-custom design

- Considerations
  - Vendor designs logic cells
  - Vendor knows process technology and physics
  - Designer works at logic (block) level
    - Schematic level design
    - Logical interconnect between functional blocks
  - Designer cannot modify internal cell design
- Tools
  - Schematic editor
  - Logic simulation (possibly multilevel)
  - Net-list generation
- Predominant semi-custom technologies
  - Gate array
  - Standard cell

Standard cell design

- CMOS circuit technology
- Characteristics
  - Full mask set is used
  - No wafer pre-processing
  - Cells are full custom design
  - Cells may be placed anywhere on chip
  - High routing flexibility
  - Cells may have fixed pitch
    - Eases routing through uniformity
    - Wiring by abutment is possible
- Advantages
  - Cell libraries
    - Correct by construction
    - Supported by CAD vendors
    - High density custom design permits complex functions
  - Conventional "block oriented" design style
  - Less space wasted due to routing
  - Smaller part size is possible due to higher density
- Disadvantages
  - Not as dense as full custom
  - More processing required due to use of full mask set
  - Lower economic return due to scale (preprocessing)
- Application
  - Controllers
  - Moderate production volume applications

Gate array design

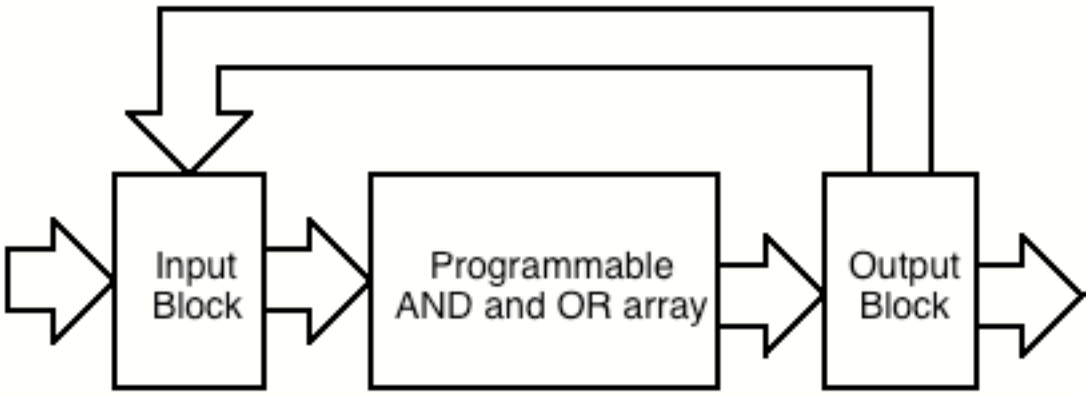
- Circuit technology
  - CMOS
  - Bipolar ECL
- Characteristics
  - Regular array of uncommitted gates
  - CMOS: rows of P and N transistors
  - Wafers are preprocessed
  - Metal layers are added later to form functions
- Variations
  - Predefined routing channels
  - Sea of gates (no routing channels)
- Advantages
  - Wafers can be pre-processed in large volume
  - Arrays are regular and simple to produce
  - Cell libraries are available
    - Well-supported by CAD vendors
    - Circuit performance is characterized and predictable
    - Cells are pretested leading to "correct" designs
  - Design style is conventional
- Disadvantages
  - Not as dense as full custom design
  - Some gates left unused due to routing problems
- Application
  - Replace random logic
  - Glue logic
  - Short fuse projects (fast turn around)
  - Low volume applications

National SCX6260 CMOS gate array

- 6000 gate array
- 2 micron feature size, 0.85 ns gate delay
- Internal matrix
  - 3953 cells (3 transistor pairs per cell)
  - 5930 2-input gate equivalents
- Input / output circuitry
  - 172 pads
  - 12 power supply pads
  - 88 birectional ports
  - 66 dedicated inputs
  - 4 test pins
  - 1 clock pin
  - 1 output disable pin
- On-chip maintenance
  - 12 percent space penalty
  - Scan in - scan out design
  - On-chip PRN pattern generation
  - On-chip signature formation
- Macros
  - Inverter
  - Buffer
  - 2-, 3-, 6-input Aand
  - 2-, 5-input And
  - 2-, 3-, 6-input Nor
  - And-Or-Invert
  - Exclusive Or, exclusive Nor
  - 2-, 4-, 8-to-1 multiplexers
  - 2to 4, 3 to 8 decoders
  - Dynamic and static flip/flops
  - 4-bit shifter, 4-bit adder, 4-bit comparator
  - Parity generation
  - 16-word RAM

Programmable logic devices (PLD)

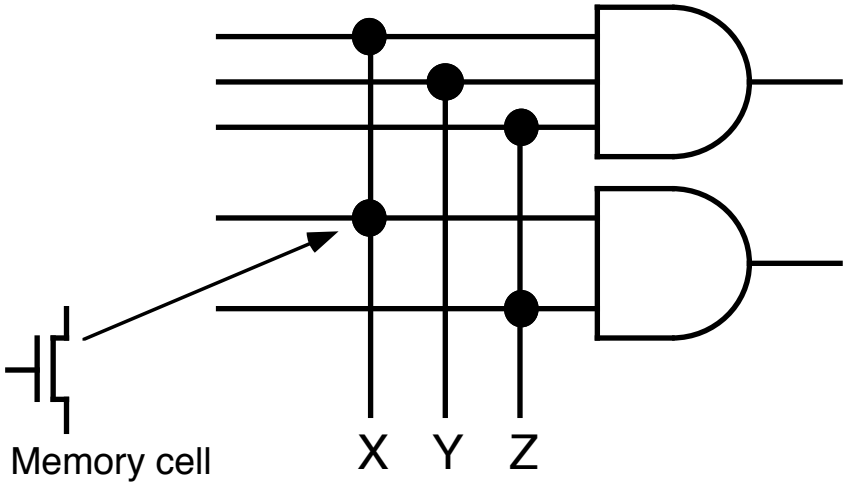
- Variation on programmable logic array (PLA)
- Two level, sum of products form
- Architectural additions
  - Input and output blocks
  - Registers
  - Latches
  - Programmable feedback (for sequential logic)



- Predetermined features
  - Number and location of AND/OR connections
  - Number of inputs and outputs
- User-defined features
  - Which connections to open or close
  - Sum of products logic (array programming)
  - Operating mode of input and output blocks

PLD technology

- Programmability through memory technology
  - Fuses
  - EPROM cells
  - EEPROM cells
  - Static RAM
- Off-the-shelf, ready to customize parts



- Bipolar fuse devices
  - Fast
  - High current consumption and power dissipation
  - 5 Volt minimum operating supply voltage
  - Fuses require large area ⇒ lower functional density
  - One-time programmable
- Erasable PLD (Intel)
  - EPROM cells using CHMOS
  - Lower power than bipolar
  - Can operate on lower supply voltages
  - Memory cells are much smaller than fuses
  - Functional density higher; chip size smaller

Intel EPLD family

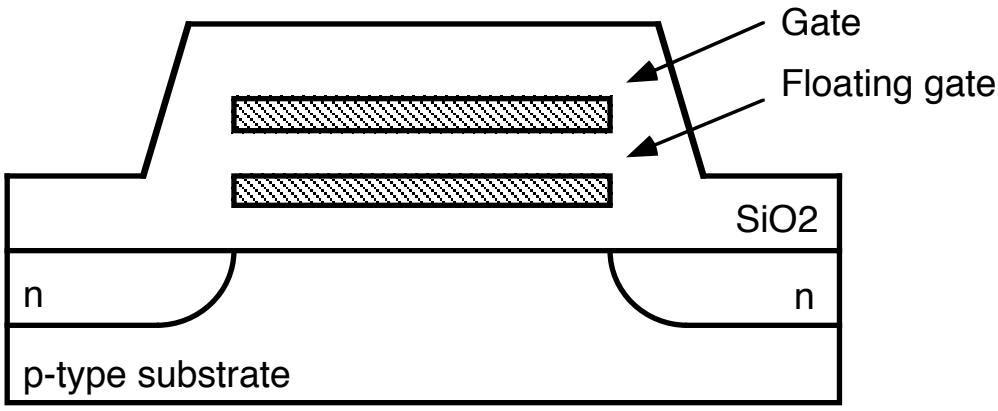
5C031	300 gates	10 in	8 i/o	40 ns
5C032	300 gates	10 in	8 i/o	25 ns
5C060	600 gates	4 in	16 i/o	45 ns
5C090	900 gates	12 in	24 i/o	50 ns
5C121	1200 gates	12 in	24 i/o	50 ns
5C180	1800 gates	16 in	48 i/o	75 ns

Intel 5C180

- 48 macrocells separated into four quadrants
- Synchronous clock input per quadrant
- Macrocell characteristics
  - 88 input AND array
  - Ten product terms to common OR gate
- Two level bus structure
  - Local bus
  - Global bus
- Four different register modes
  - D-type flip/flop
  - T-type flip/flop (toggle)
  - JK-type flip/flop
  - SR flip/flop
- Erasure
  - Exposure to light with less than 4000 A wavelength
    - Flourescent lighting - erasure in three years
    - Direct sunlight - erasure in one week
  - Shortwave UV light (2537 A wavelength)
    - Integrated dose = intensity $\times$ time
    - 20 minutes at 12,000 $\mu W / cm^2$
    - Overexposure can cause permanent damage

Erasable Programmable ROM

- Nonvolatile memory
- Intel floating-gate, avalanche-injection MOS (FAMOS)
- Floating gate is electrically isolated by silicon dioxide



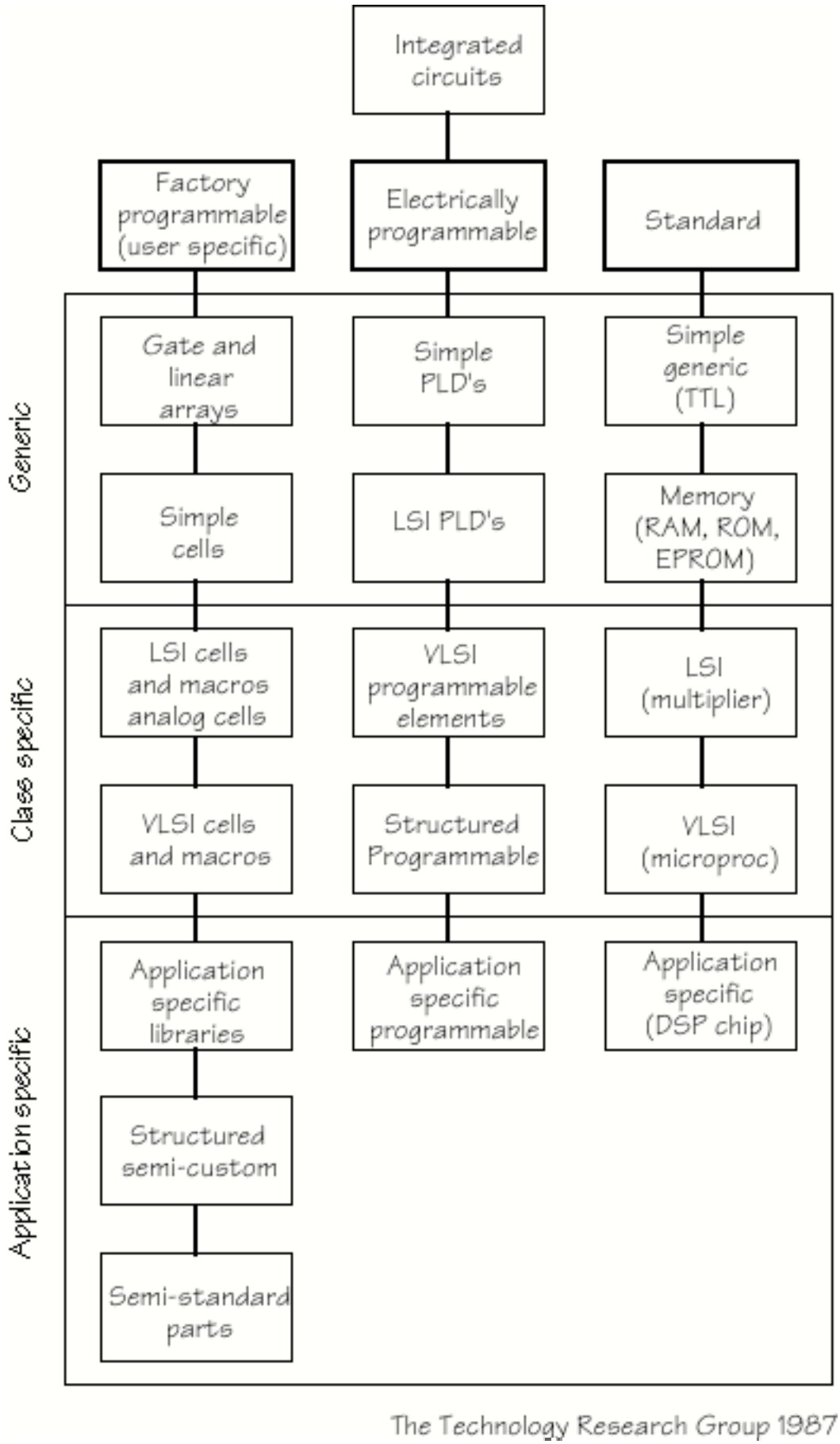
- Erase operation
  - Expose memory cells to UV light
  - Stored electrons on floating gate become excited
  - Electrons discharge to ground (via substrate)
  - All cells are set to "0" (no stored charge)
- Write operation
  - Apply high voltage (25 - 40V) to gate to write a "1"
  - Electrons enter floating gate from substrate
- Storage
  - Absence and presence of charge ⇒ "0" and "1"
  - Electrons remain stored on the isolated gate
  - Some charge leakage does occur
  - Retention time is "tens of years"
- Read operation
  - Positive charge on gate is masked by electrons
  - 0 (1) ⇒ channel is conductive (nonconductive)

Xilinx Logic Cell™ Array

- Programmable array of logic cells
  - Serially download programming information
  - XC3020 array
    - 2000 usable gates
    - 64 configurable logic blocks
    - 58 user input/output pins
    - 14815 program bits
  - Static CMOS memory cells for control
- Structure
  - I/O blocks (IOB) on perimeter of chip
    - Latched and direct input
    - Clamping diodes for electro-static protection
    - Input thresholding for TTL or CMOS levels
    - Latched and direct output
    - High fanout CMOS and TTL output levels
    - Three state output selectable
  - 8 by 8 array of configurable logic blocks (CLB)
  - CLB's are surrounded by connection network

Technology	Wafer preprocessing	Cost of prototype	Time to prototype
Full custom	0%	$50K - 250K	9-18 months
Standard cell	0%	$30K - 90K	4 - 6 months
Macro cell	80%	$15K- 40K	3 - 4 months
Gate array	80-90%	$5K - 20K	1 - 2 months
Programmable	100%	At cost	off the shelf

Technology	Density	Speed	Prog'ability
Full custom	Very high	Very high	Low
Standard cell	High	High	Low
Macro cell	Moderate	High	Moderate
Gate array	Moderate	High	Moderate
Programmable	Low	Moderate	High



Example: DSP system

- FIR filter
- Very specific algorithm (application)
- Audio processing is slow, video is very fast

Technology	Example	Cost	Time
Full custom	CMOS	$150K	10 months
Standard cell	Toshiba	$60K	4 months
Gate array	Toshiba	$27K	3 months
FPGA	Xilinx	$50	2 months
PLD	Intel EPLD	$40	2 months
DSP processor	M56000	$300	2 months
ASIC	LSI Logic	$450	2 months

Technology	Turnaround	Gates	Clock
Full custom	4 weeks	400,000	40MHz
Standard cell	4 weeks	70,000	40MHz
Gate array	1 week	50,000	30MHz
FPGA	1 hour	6,000	20MHz
PLD	1 hour	2,000	20MHz
DSP processor	15 minutes	Software	N/A
ASIC	WYSIWYG	N/A	16MHz

- What approach has the lowest risk?
- Which solution has the smallest package count?
- Is very high performance necessary?
- How many systems will be sold?
- Can proprietary algorithms be protected?