VLSI design

Introduction to CMOS circuits

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Digital circuit technology

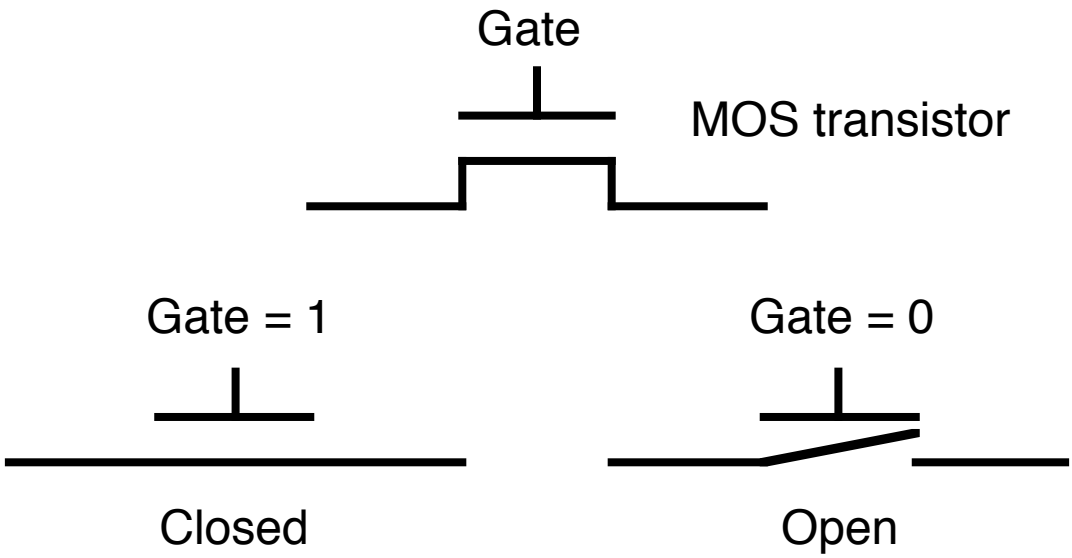
- Representation
- Decision and computation
- Storage (memory)
- Energy loss

Binary representation

- Absence/presence of charge
- Example
  - Absence = "0" (0 Volts)
  - Presence = "1" (+5 Volts)

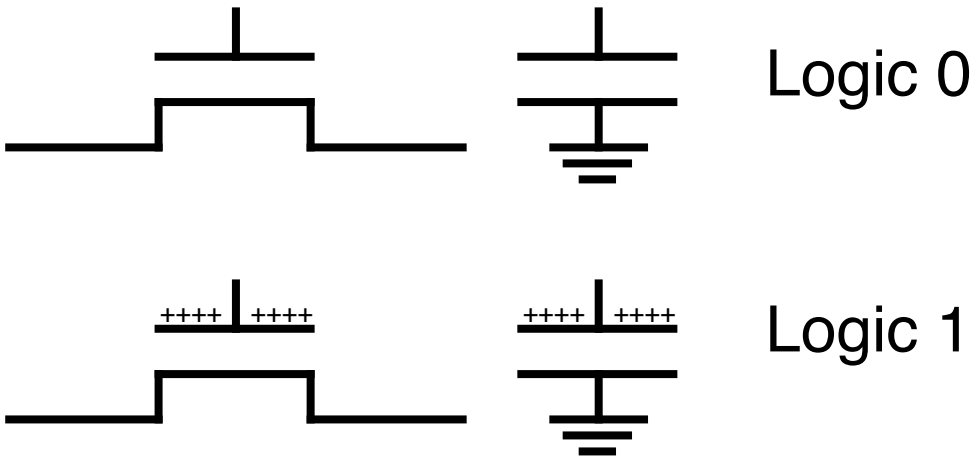
Decision and computation

- Charge (voltage) controlled switch
- Example: MOS transistor switch



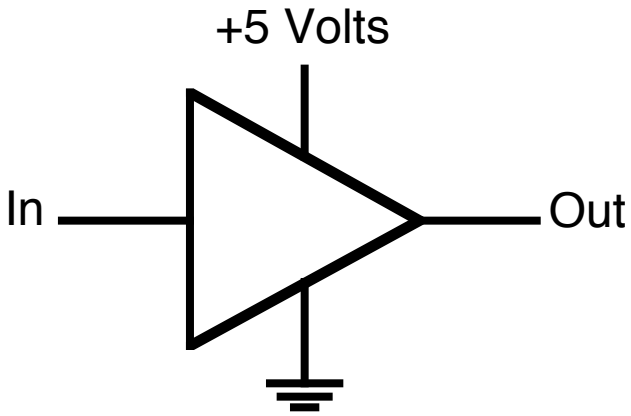
Information storage

- Capacitor (charge storage)
- Example: MOS transistor

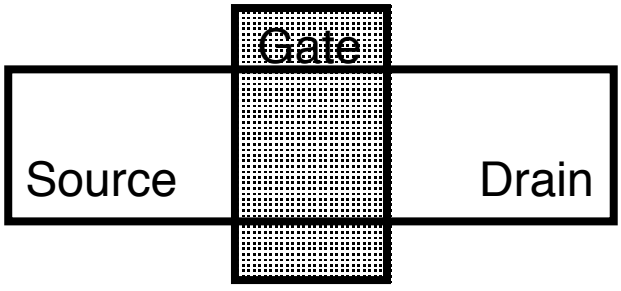


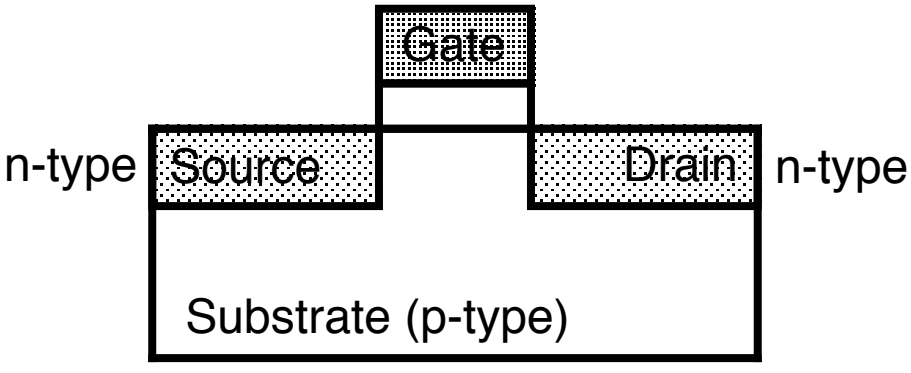
Energy loss

- Restoring logic
- Amplification
- Power supply

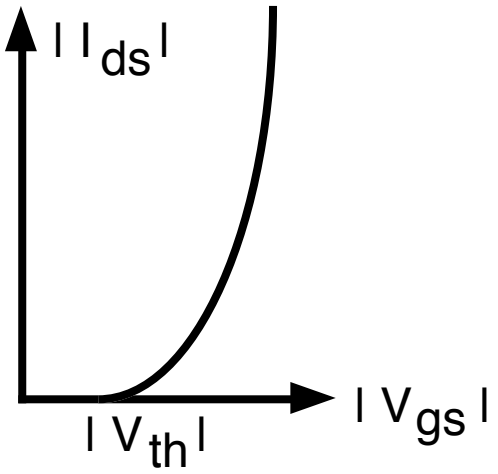


Simplified transistor structure

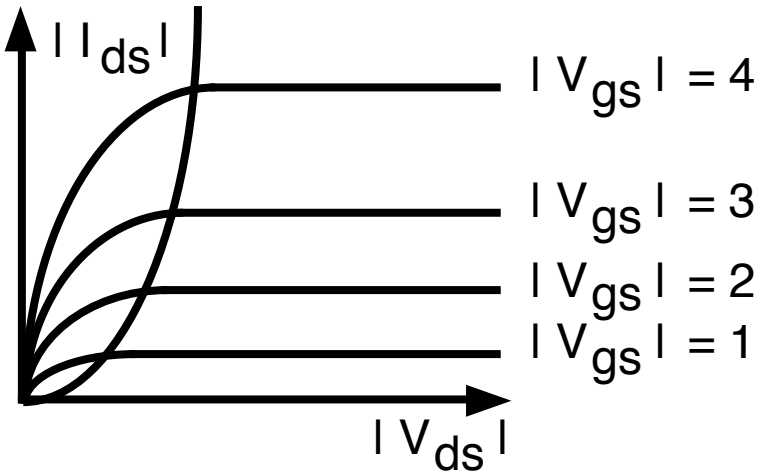




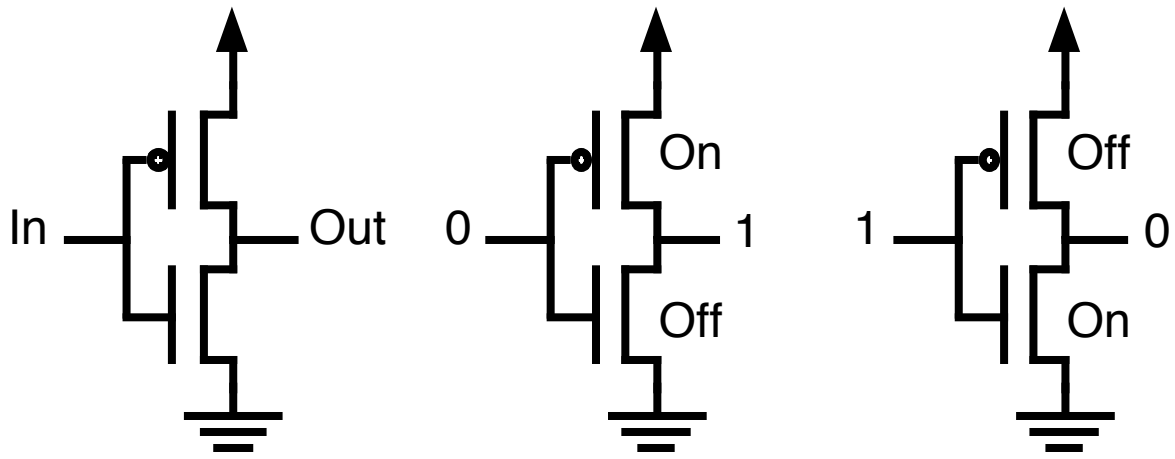
Vgs vs. Ids



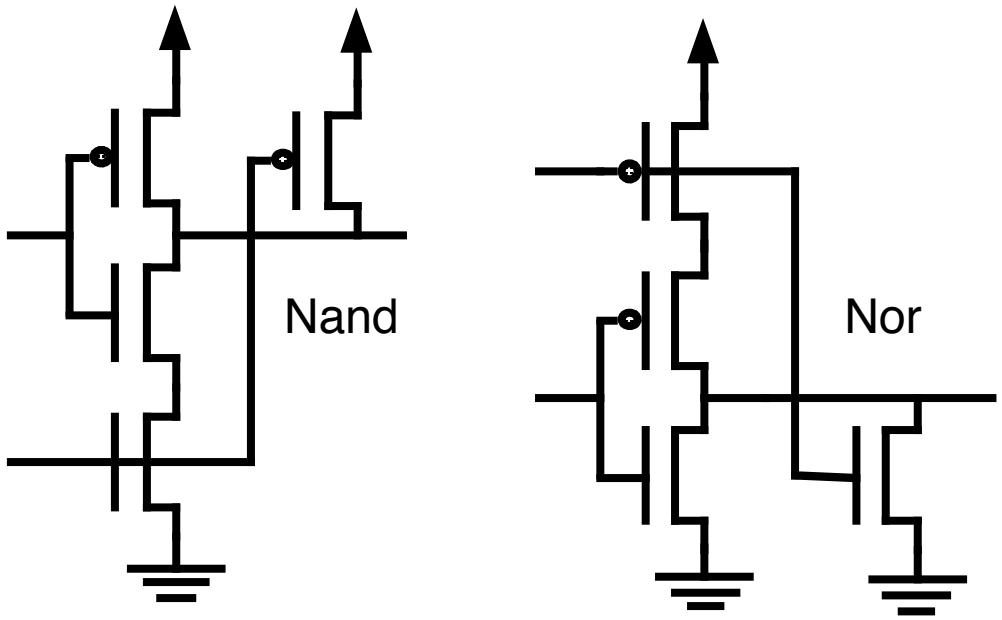
Vds vs. Ids



CMOS inverter



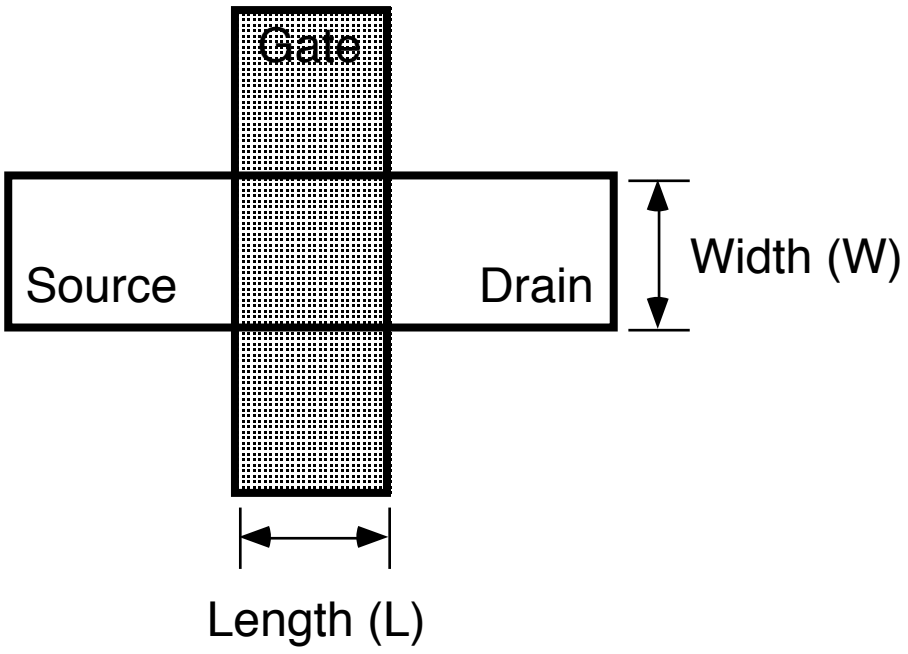
CMOS logic gates



Choosing transistor sizes (W and L)

- Delay
  - Rise time
  - Fall time
- Current consumption
- Power dissipation

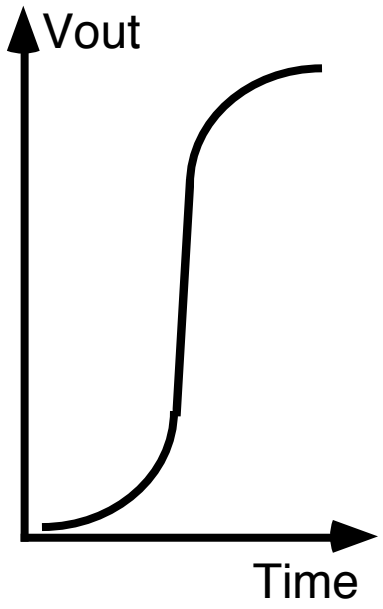
Channel width and length



Rise time

- Time to rise from 10% to 90% of final value.
- Pull-down transistor is off.
- Pull-up channel and load form an RC circuit.

$$\text{Trise} = 4\,\frac{\text{Cload}}{\beta \times \text{Vdd}} \qquad \beta = \frac{\mu \times \varepsilon}{\text{Tox}}\,\frac{W}{L}$$

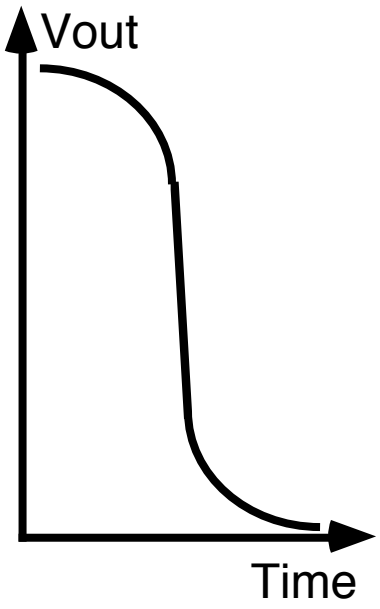


$\varepsilon = 35 * 10^{-14}$ F / cm	Permittivity of gate oxide
$\mu = 1000$ cm^2 / V-sec	Hole surface mobility
Tox = 5 microns	Thickness of gate oxide

Fall time

- Time to fall from 90% to 10% of final value.
- Pull-up transistor is off.
- Pull-down channel and load form an RC circuit.

$$T_{fall} = 4 \frac{C_{load}}{\beta \times V_{dd}} \qquad \beta = \frac{\mu \times \varepsilon}{T_{ox}} \frac{W}{L}$$

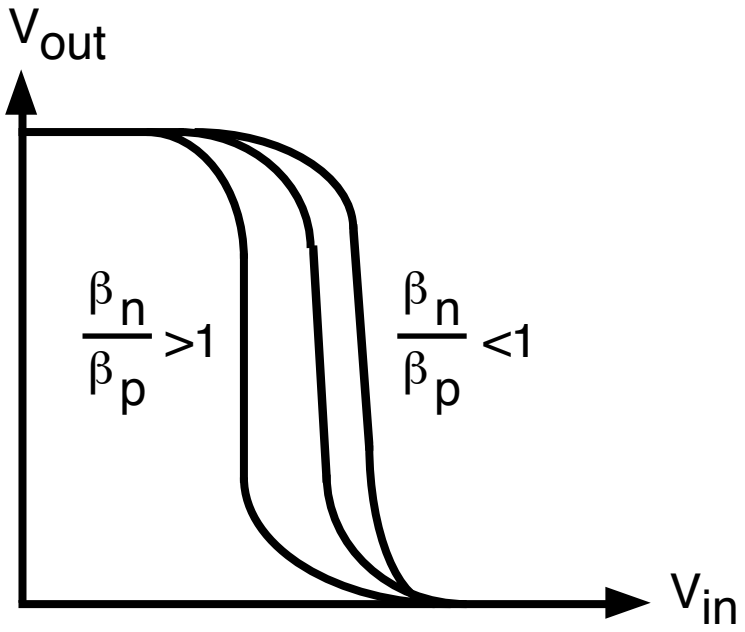


$\varepsilon = 35 * 10^{-14}$ F / cm	Permittivity of gate oxide
$\mu = 500$ cm^2 / V-sec	Electron surface mobility
Tox = 5 microns	Thickness of gate oxide

Effect of dissimilar beta values

- $\beta_n = 2 \times \beta_p$
- Then, Tfall = $\frac{\text{Trise}}{2}$
- For symmetric rise and fall, $\frac{\beta_n}{\beta_p} = 1$
- Therefore, $W_p = 2 \times W_n$

Effect on DC transfer characteristics



Static power dissipation

$$P_S = \sum_{1}^{n} \text{leakage current} \times \text{supply voltage}$$

- n is the number of devices
- Supply voltage is typically +5 Volts
- Leakage current is 0.1nA to 0.5nA per gate (25° C)
- Lower supply voltage ⇒ lower dissipation!

Dynamic power dissipation

$$P_d = C_{load} \times V_{dd}^2 \times f$$

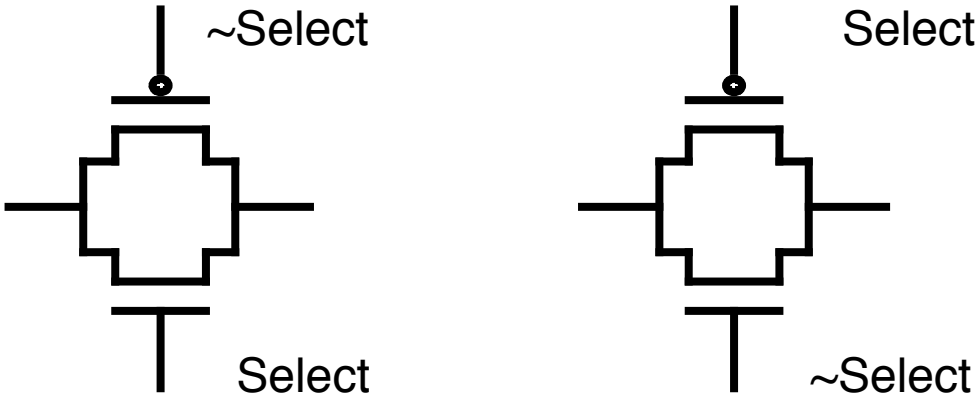
- During transitions (0⇒1, 1⇒0), both transistors are ON
- Short current pulse from Vdd to ground
- Current is required to (dis)charge load capacitance

Total power dissipation

$$P_{total} = P_s + P_d$$

- Portions of design may operate at different frequencies

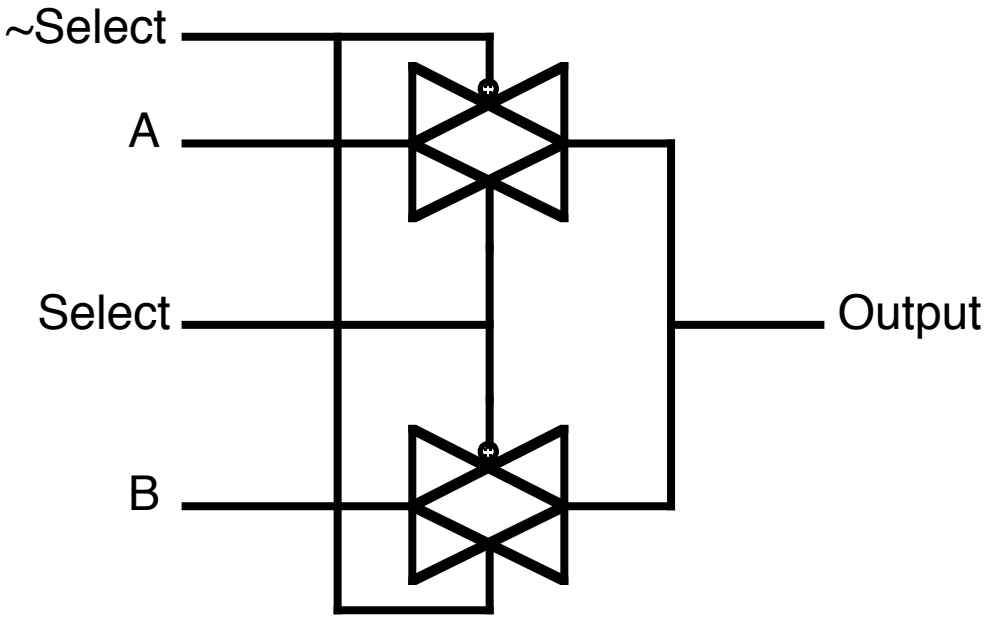
CMOS transmission gate



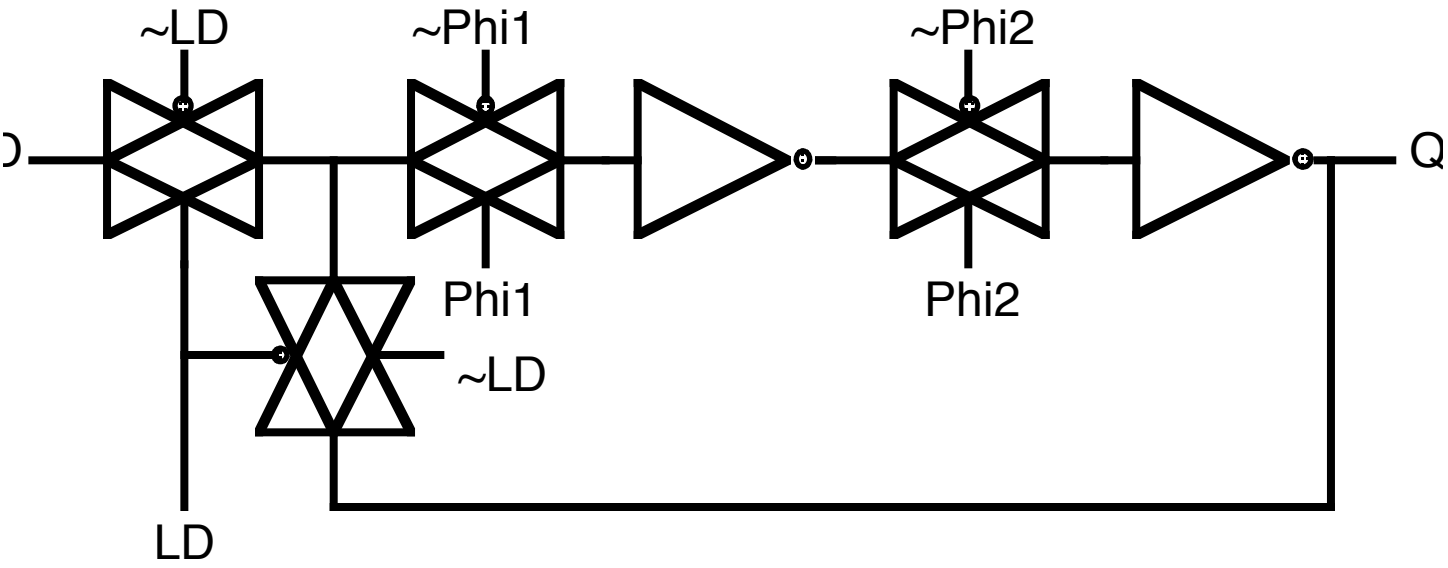
Normally open

Normally closed

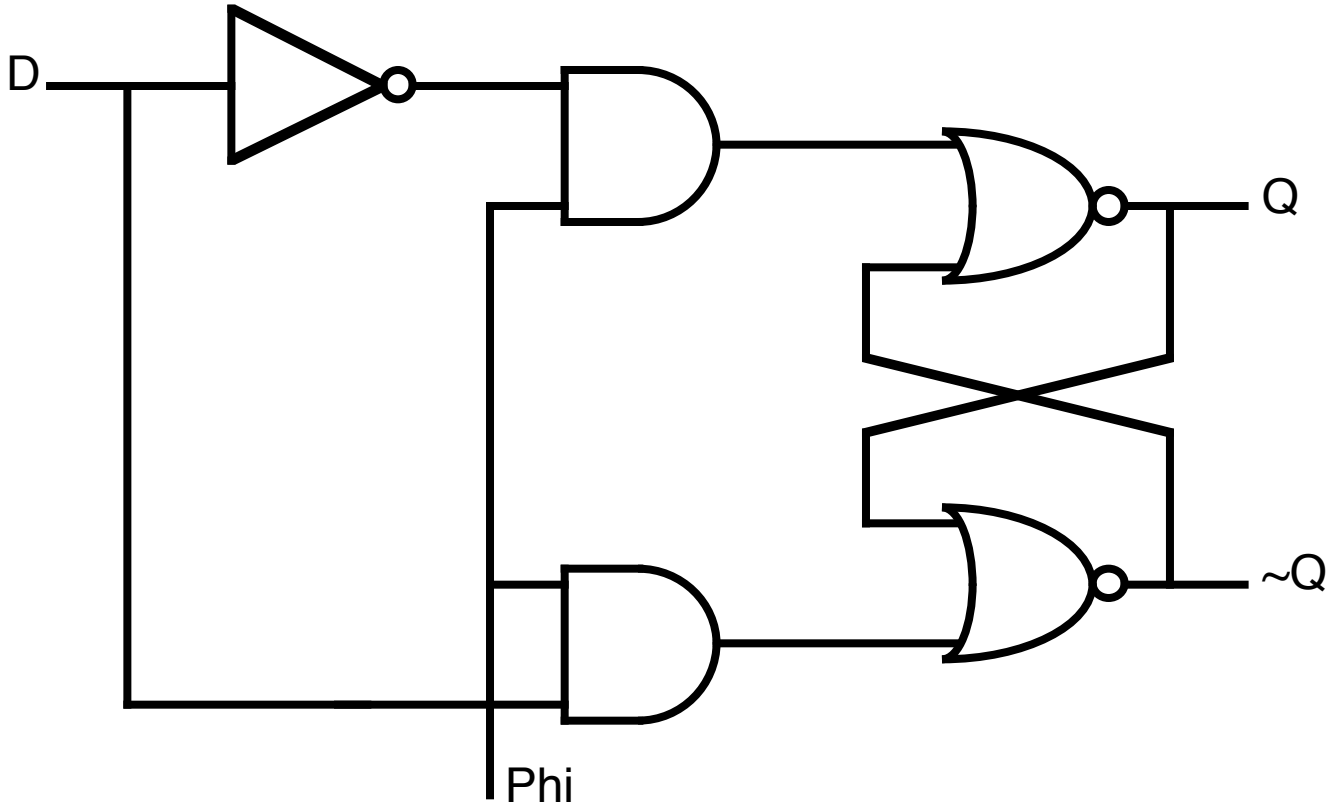
CMOS multiplexer



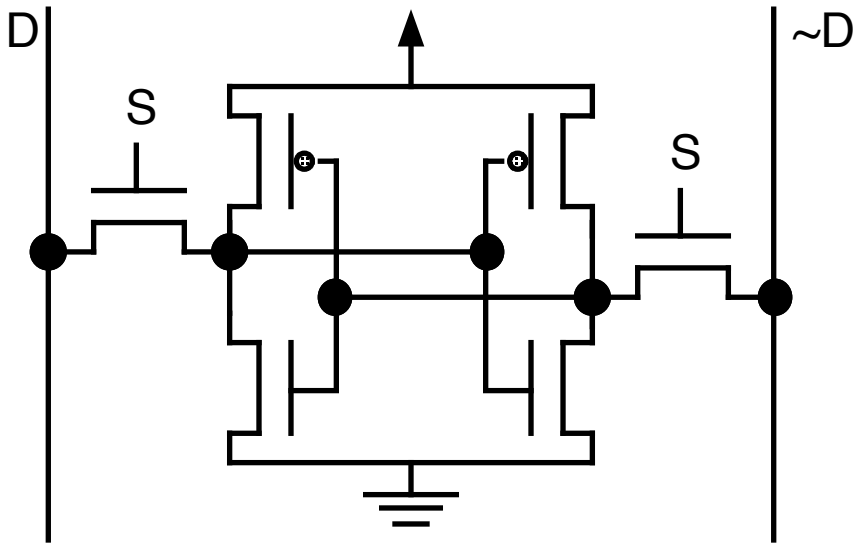
CMOS dynamic D latch



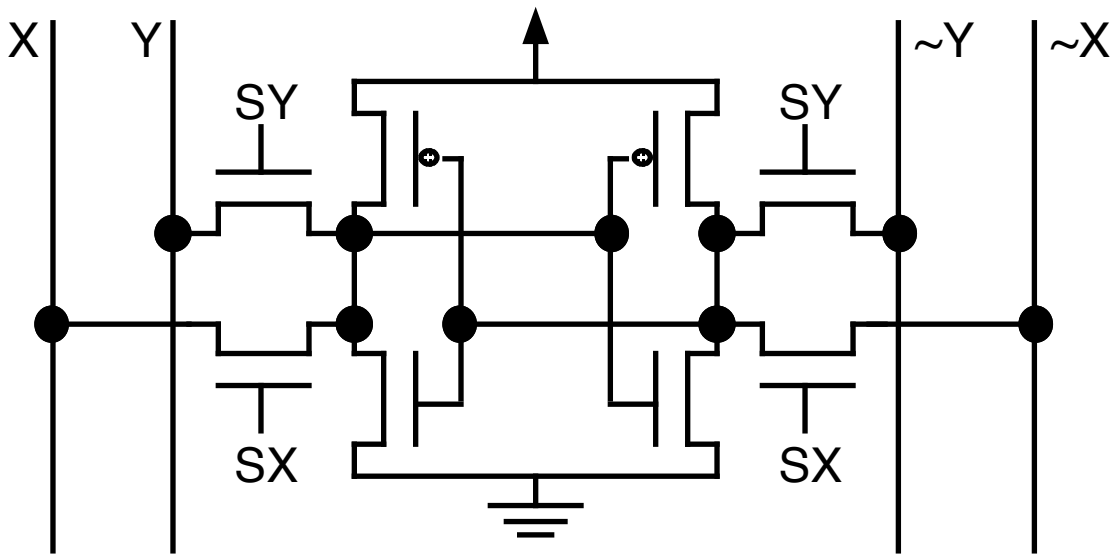
CMOS static D latch



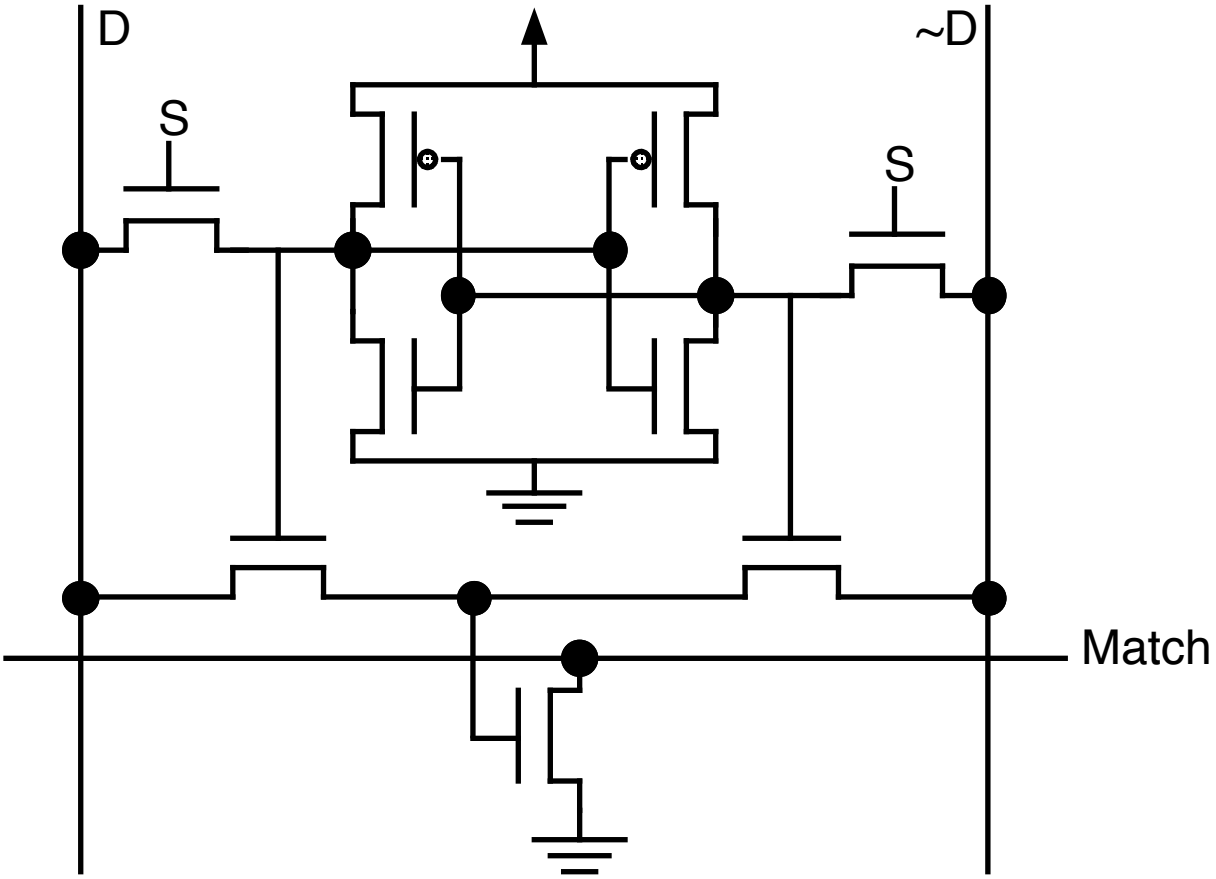
Static CMOS RAM



Dual port RAM



CMOS content addressable memory

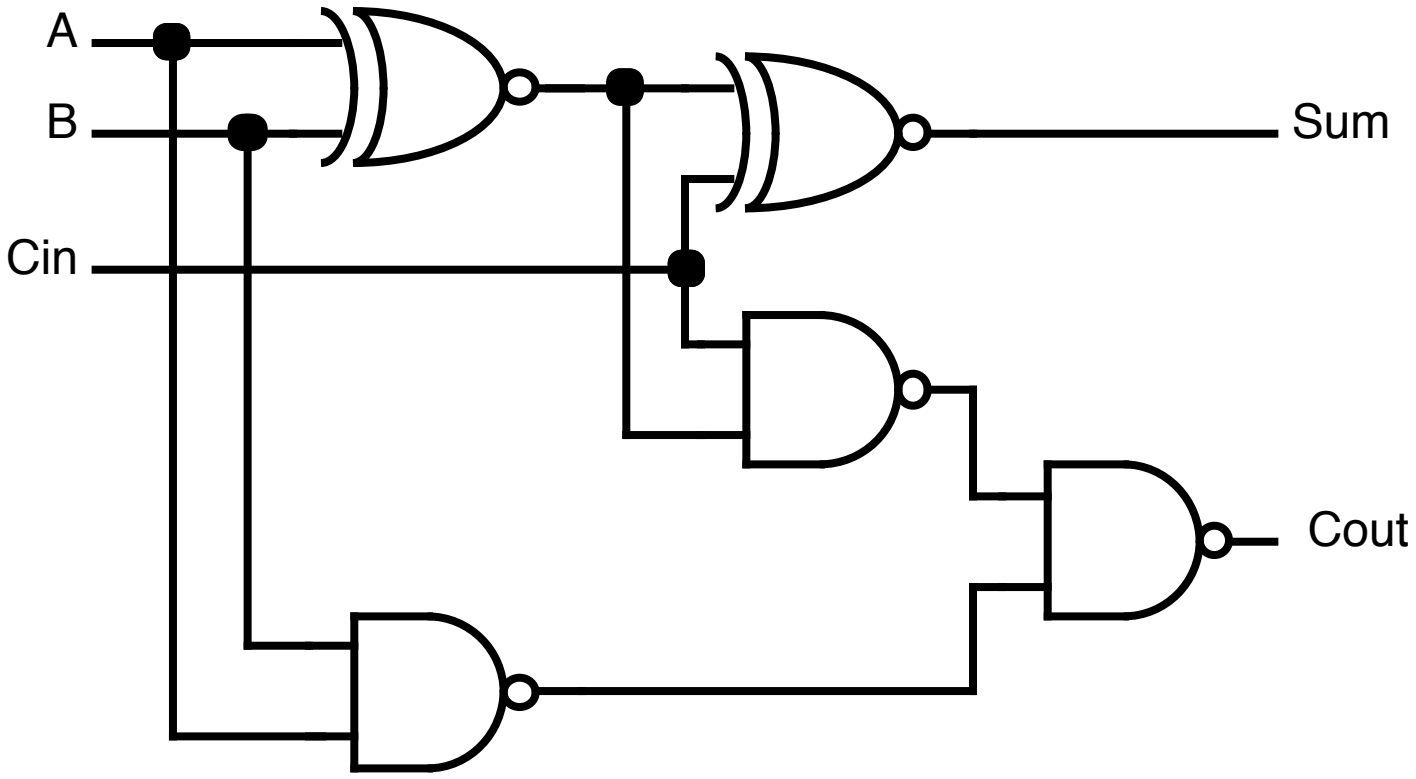


- Write operation
  - Place D and ~D on data lines
  - Assert the select line S
- Read operation
  - Precharge D and ~D lines
  - Assert select lines
  - Either D or ~D will be pulled down
- Compare operation
  - Precharge match line
  - Put pattern data on ~D
  - Put complement of data on D
  - If data matches, pull-down will remain OFF
  - If data does not match, match line is pulled down

Binary full-adder

A	B	C	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

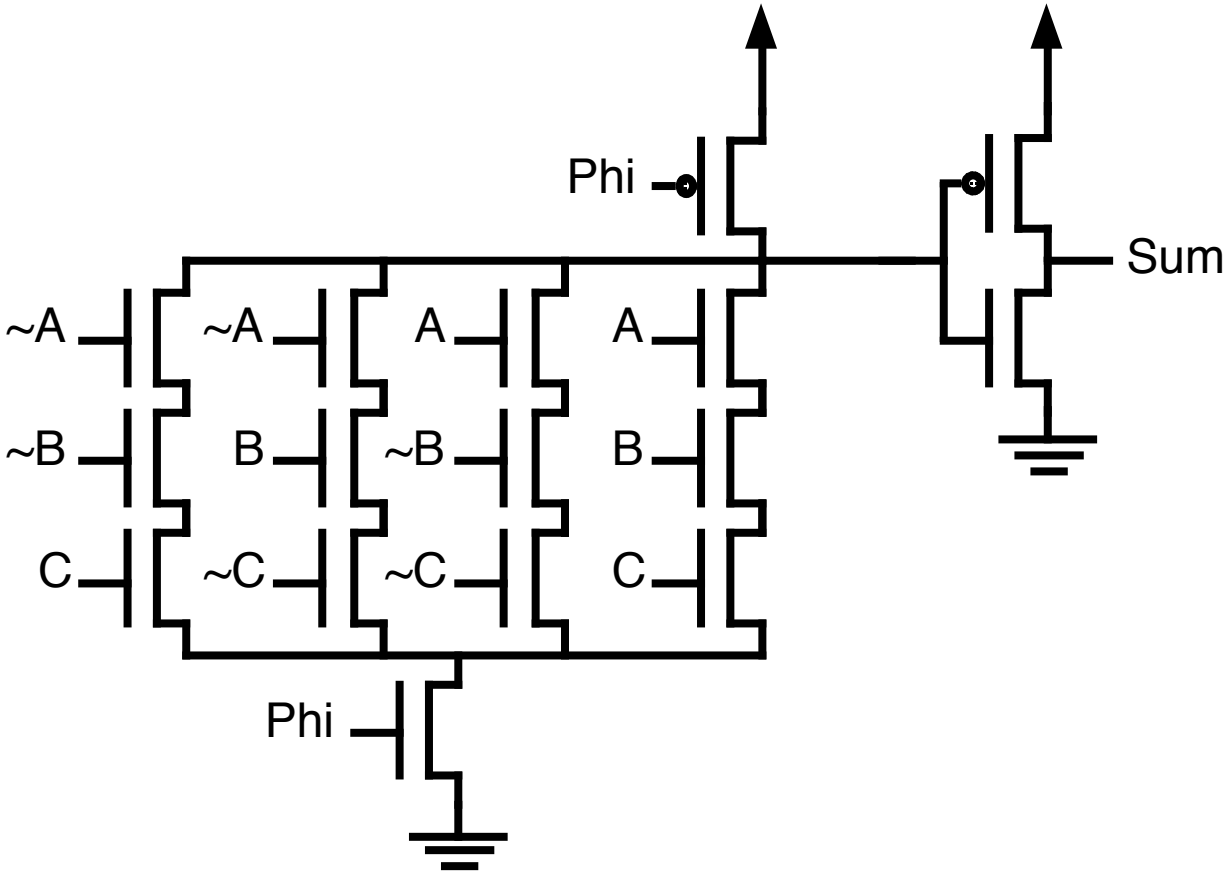
NAND and XOR implementation



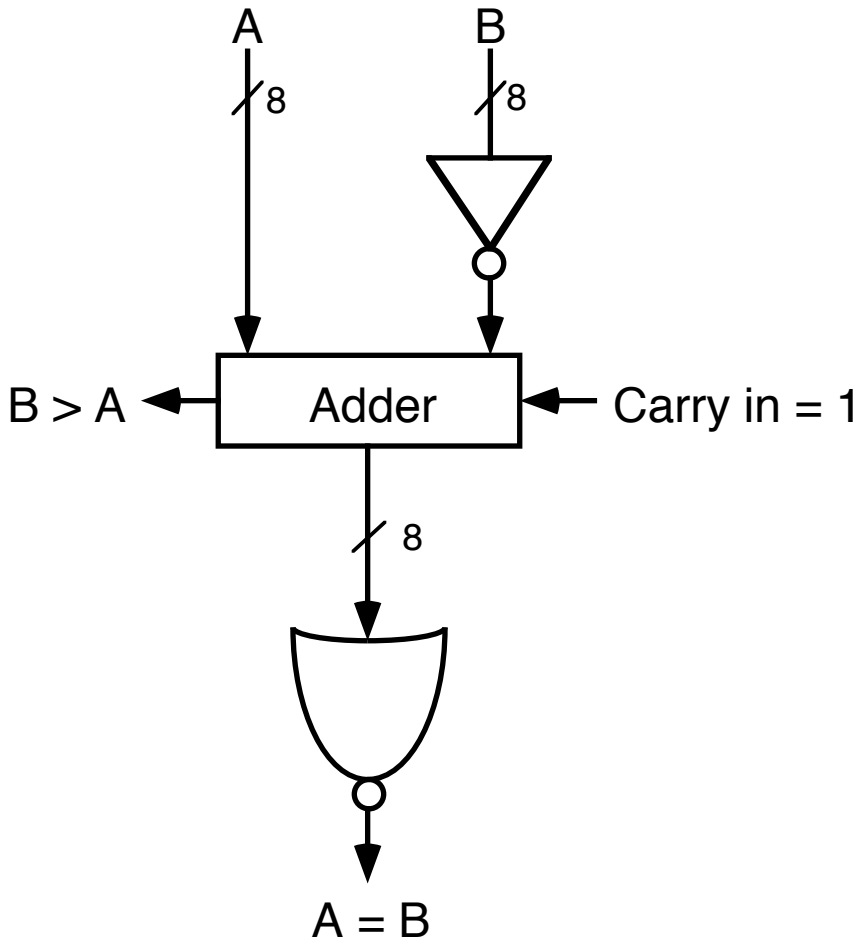
Domino logic

- Clocked CMOS combinational logic
- Add CMOS buffer to output of each logic stage
- Precharge dynamic gate high (Phi = 0)
- Conditionally discharge during evaluate (Phi = 1)
- Dynamic gate can only transition from 1 to 0
- Output of buffer only transitions from 0 to 1
- Cascaded logic evaluates and "falls" in turn
- Limitations
  - Only non-inverting logic is possible
  - Each gate must be buffered
  - Charge distribution in large structures

CMOS domino sum



Compare



Material

- Capacitance (λ = 1.5 μm)
  - Unit is capacitance per square micron of area
  - Compute area and multiply by material constant

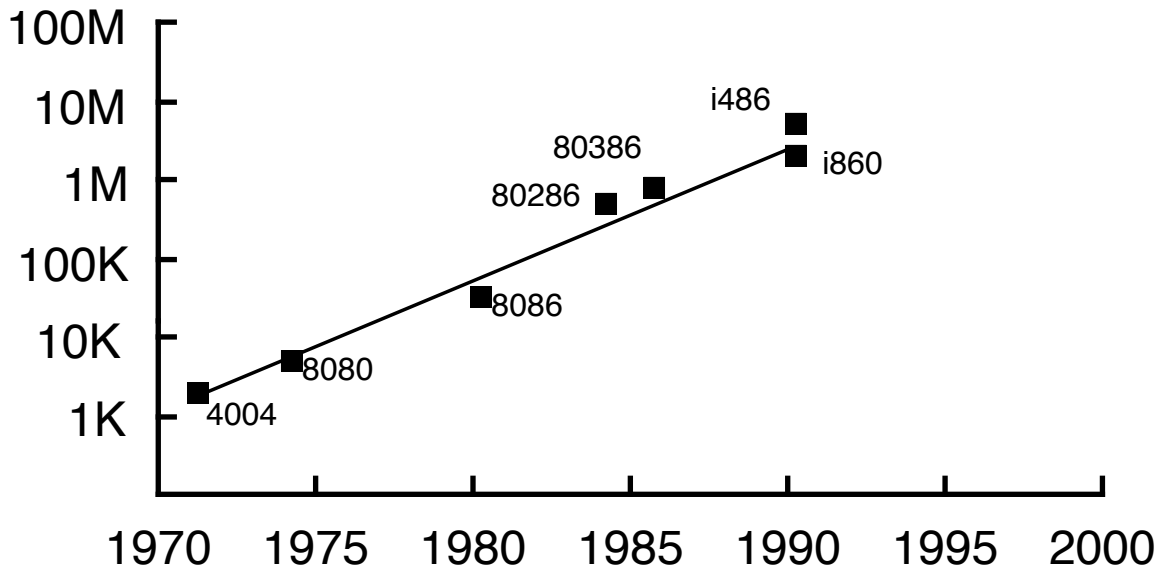
Gate	4.5×10^{-4}	pF / μm^2
Polysilicon over field	0.5×10^{-4}	
n-diffusion (active)	0.9×10^{-4}	
p-diffusion (active)	0.9×10^{-4}	
Metal 1 over field	0.2×10^{-4}	
Metal 2 over field	0.1×10^{-4}	

- Resistance
  - Sheet resistance
  - Count number of squares of material
  - Multiply by material constant
  - Resistance $R = \frac{\rho}{t}\frac{L}{W}$

ρ = Resistivity
t = Thickness
L = Conductor length
W = Conductor width

Metal	0.5 Ohms / square
Silicides	3 Ohms / square
Diffusion	25 Ohms / square
Polysilicon	50 Ohms / square

Growth of complexity



Processor	Transistors
4004	2,300
8080	6,000
8086	29,000
80286	134,000
80386	275,000
i860	1,000,000
i486	1,200,000

Microcomputer Solutions, Intel Corporation, 1989.