VLSI design

CMOS design rules

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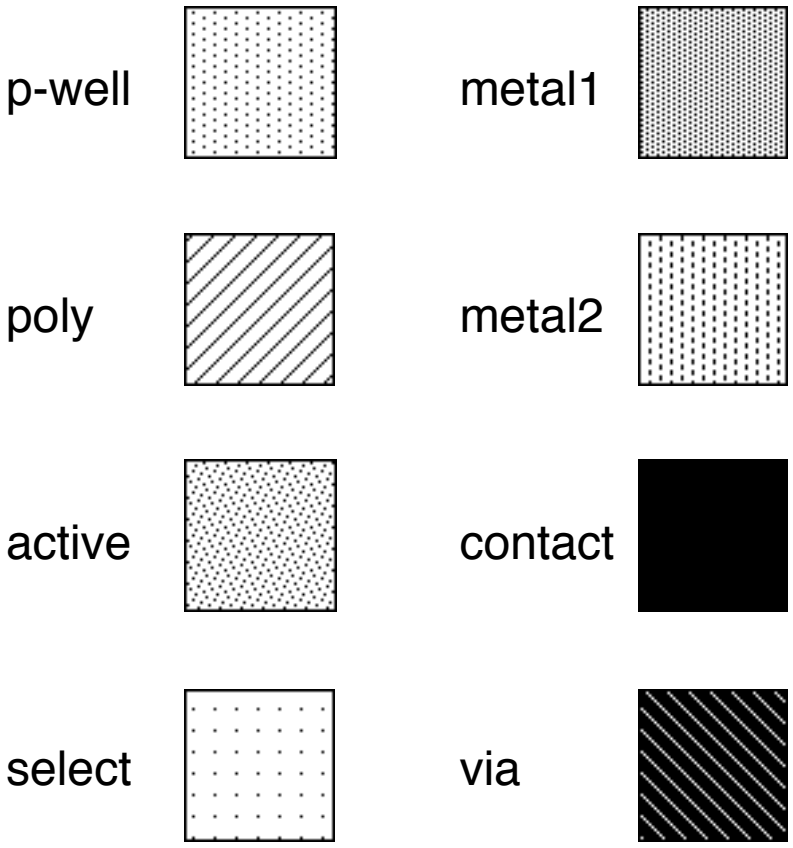
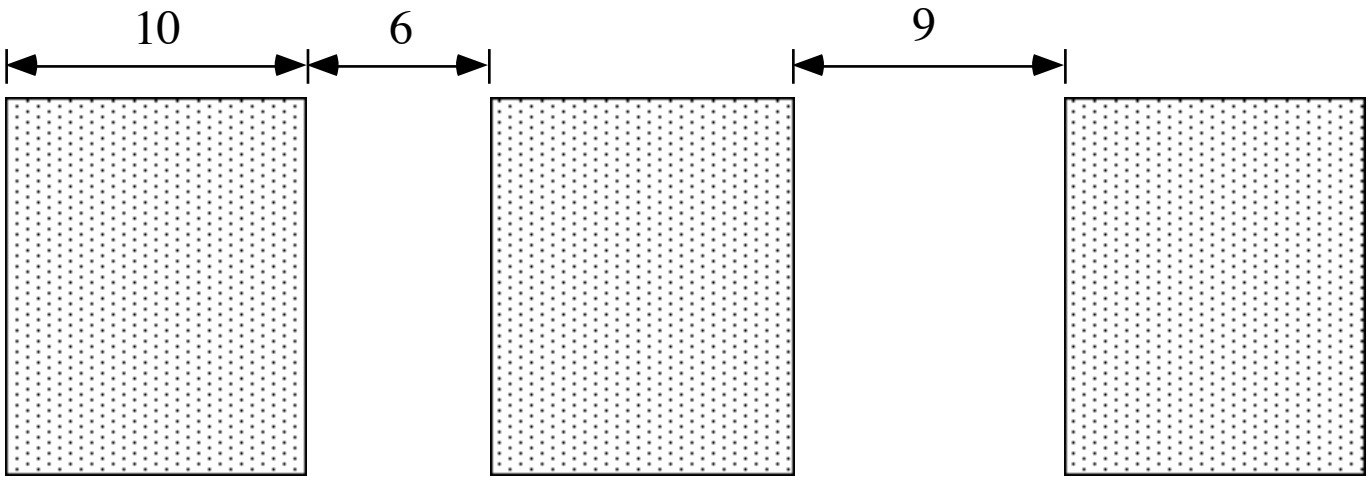
CMOS stipple patterns



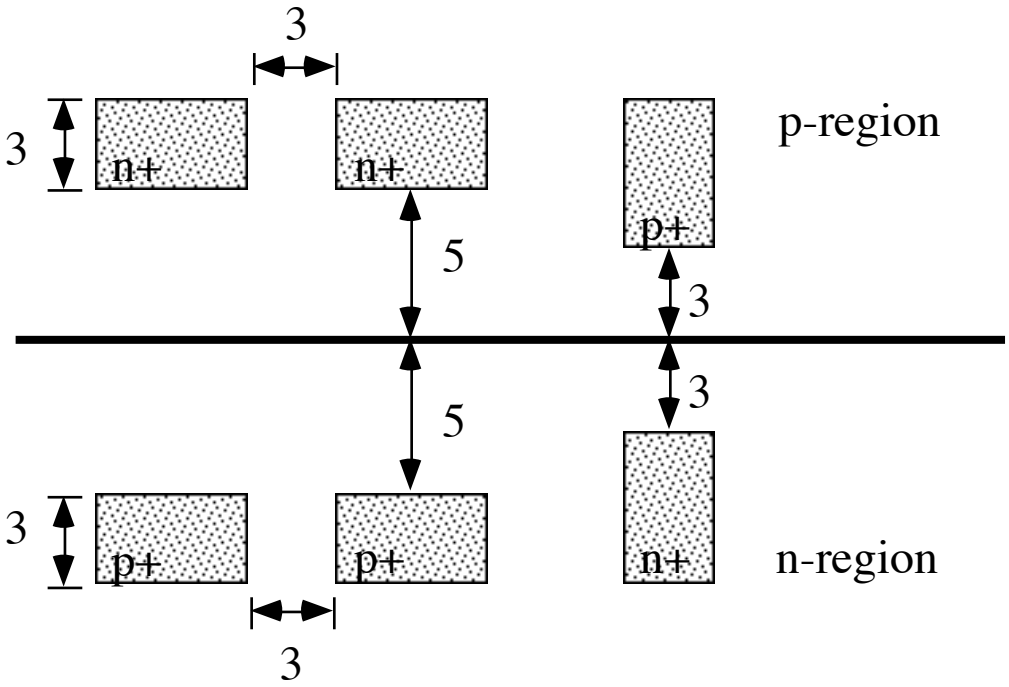
- Patterns correspond roughly to Magic
- Active is both n+ and p+ drains and sources
- Select mask chooses p-channel transistors
- Colors

Polysilicon	Red
Active	Green
Select	Yellow
Metal 1	Blue
Metal 2	Violet
Contact	Black
Via	Black cross (or brown)

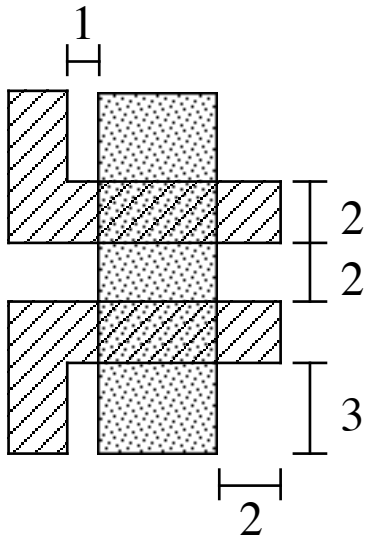
P-well rules



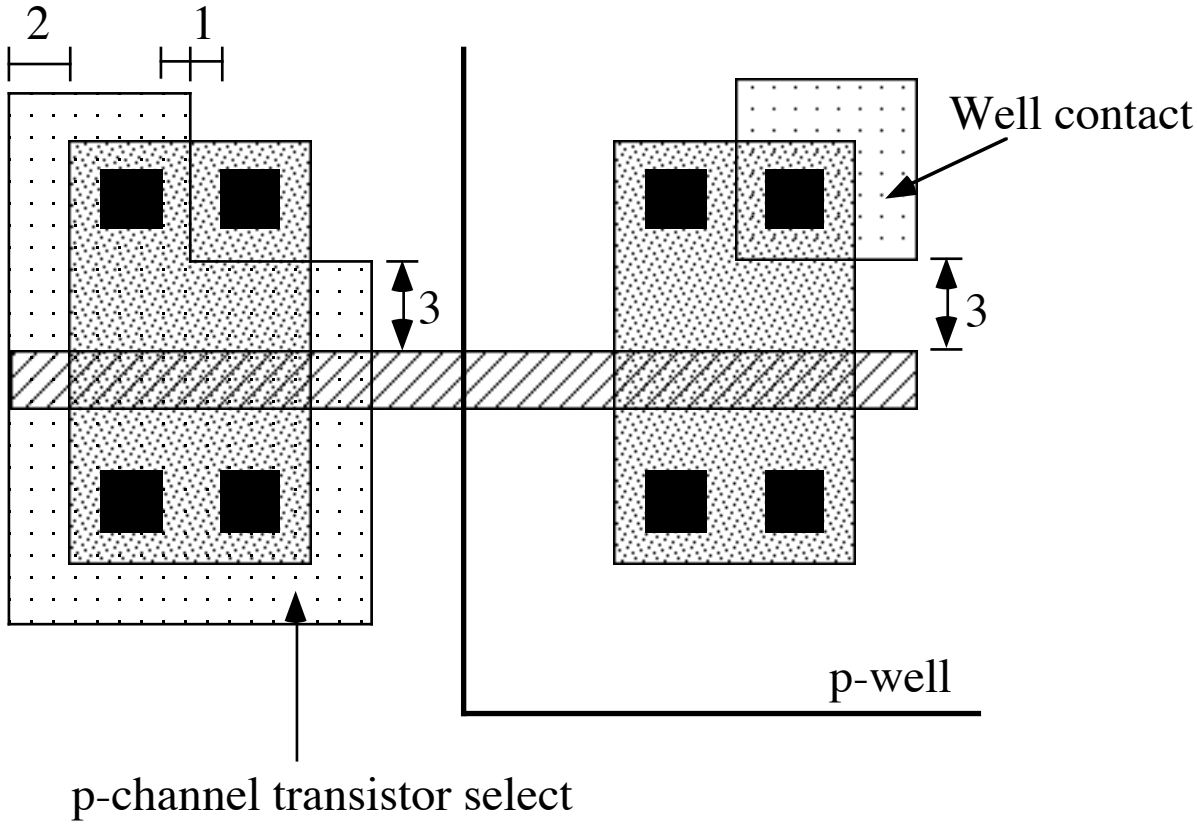
Active



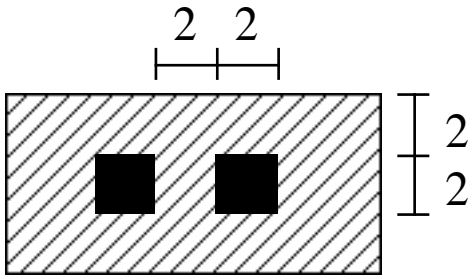
Polysilicon



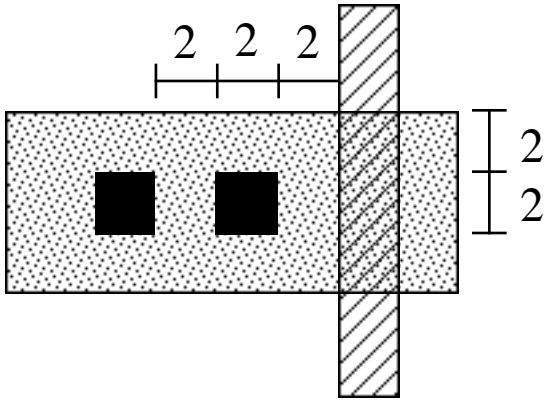
Select (p-select)



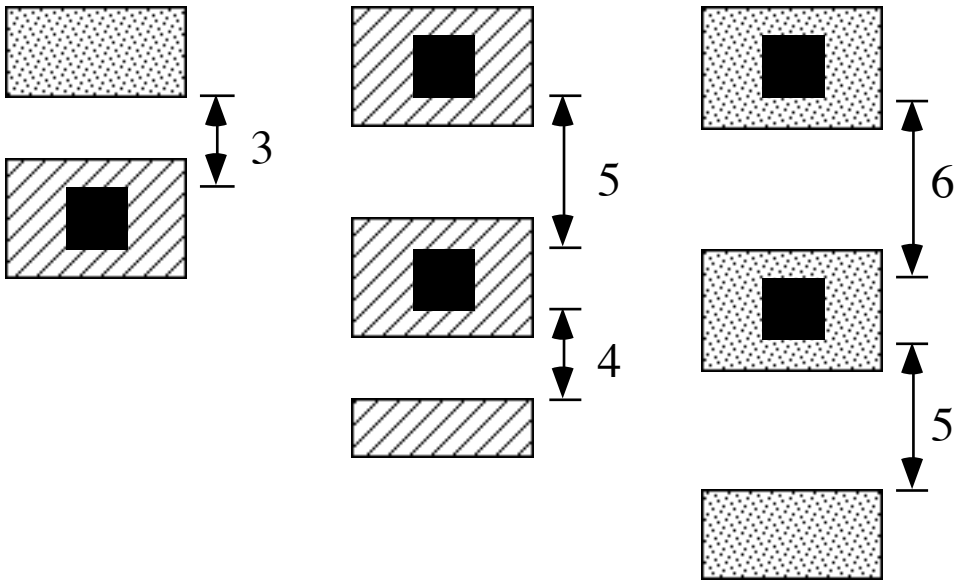
Contact to poly



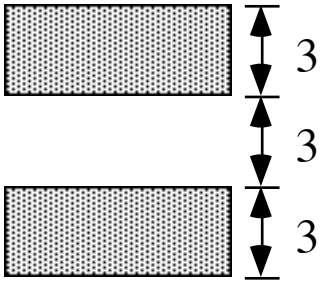
Contact to active

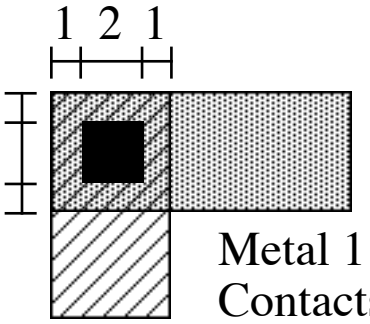


Contact to (un)related material

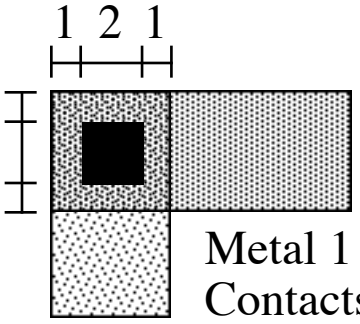


Metal 1



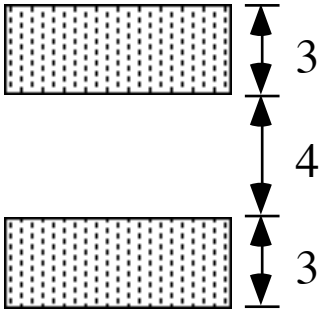


Metal 1 to poly
Contacts are 2 by 2



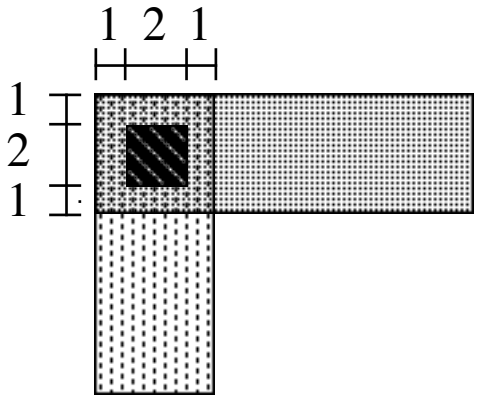
Metal 1 to active
Contacts are 2 by 2

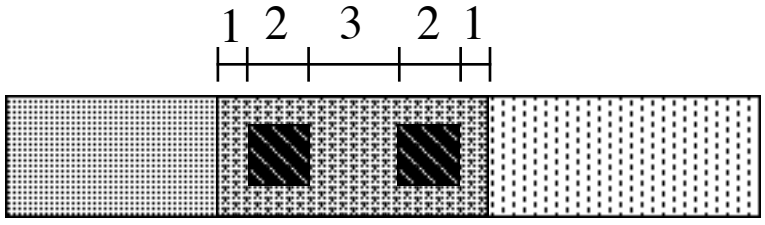
Metal 2

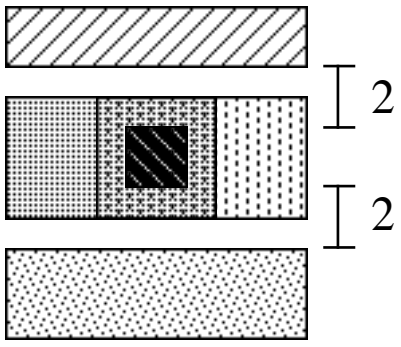


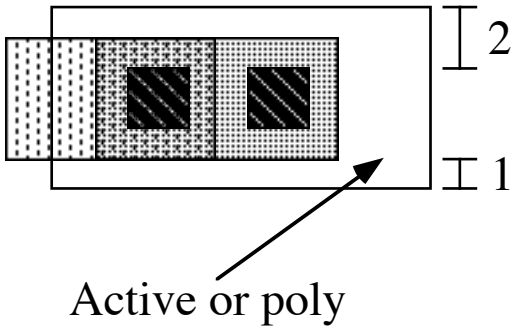
Metal 1 to metal 2 contact via
No connection to active or poly

Via (metal to metal contact)

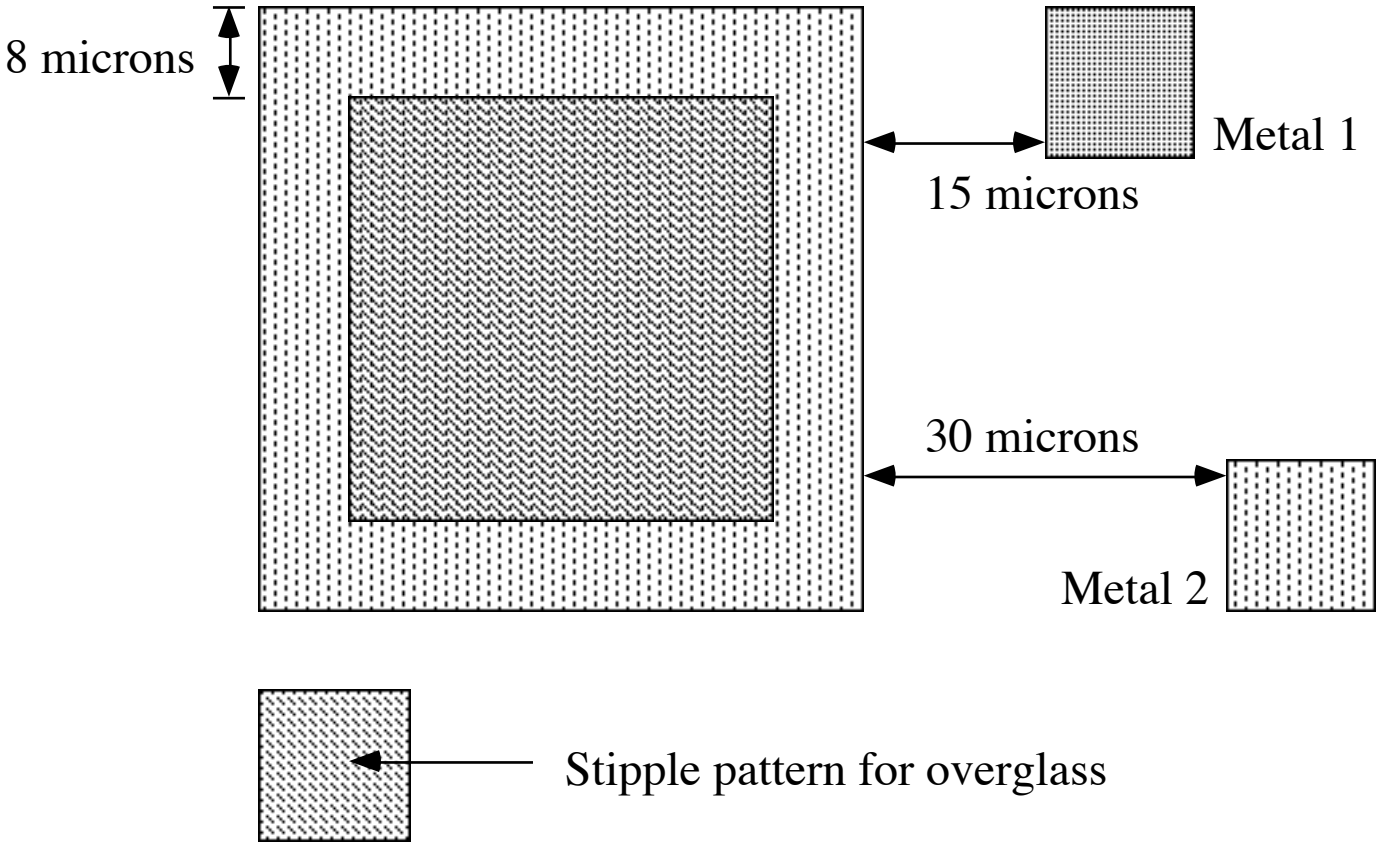






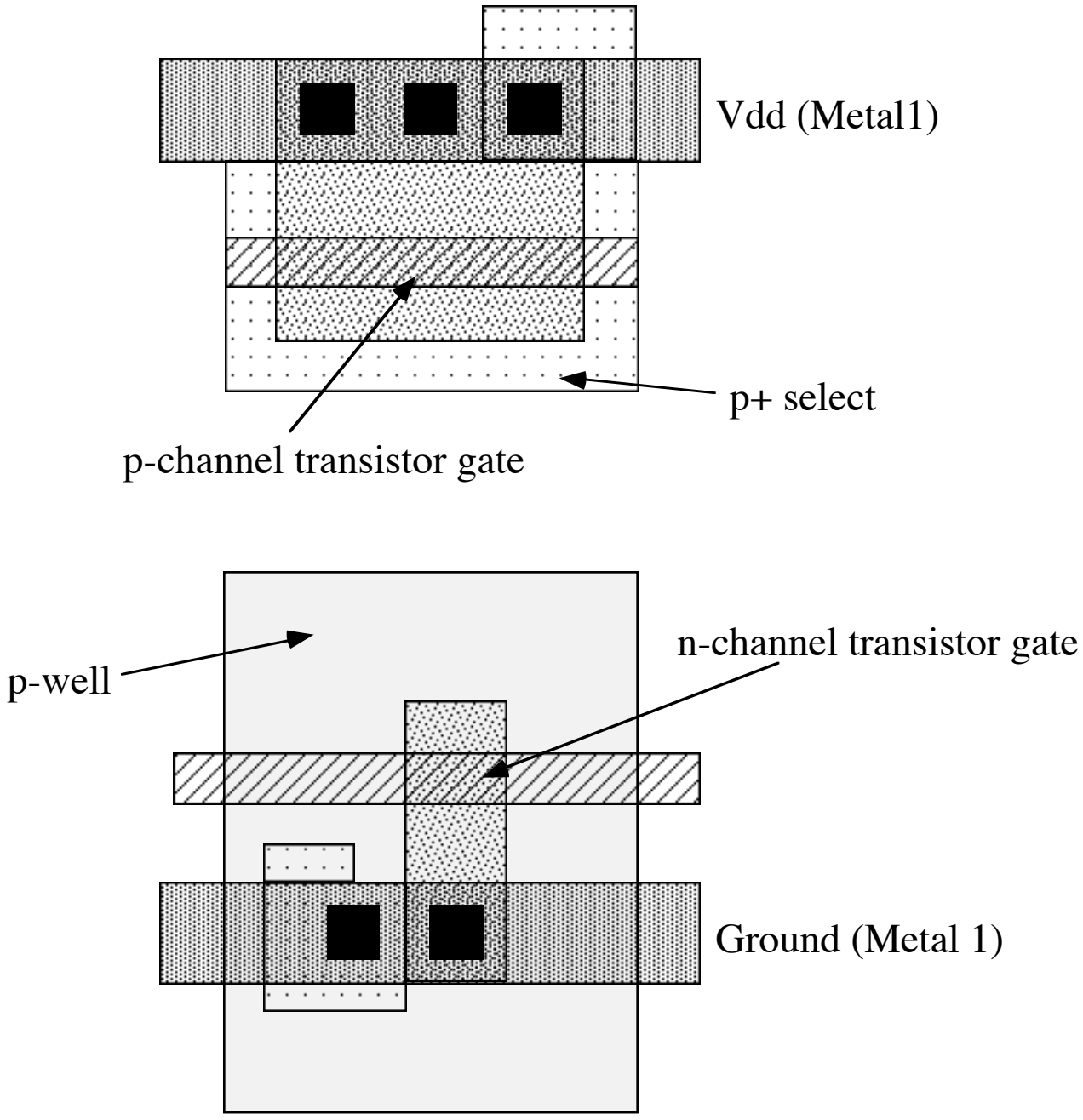


Bonding pad

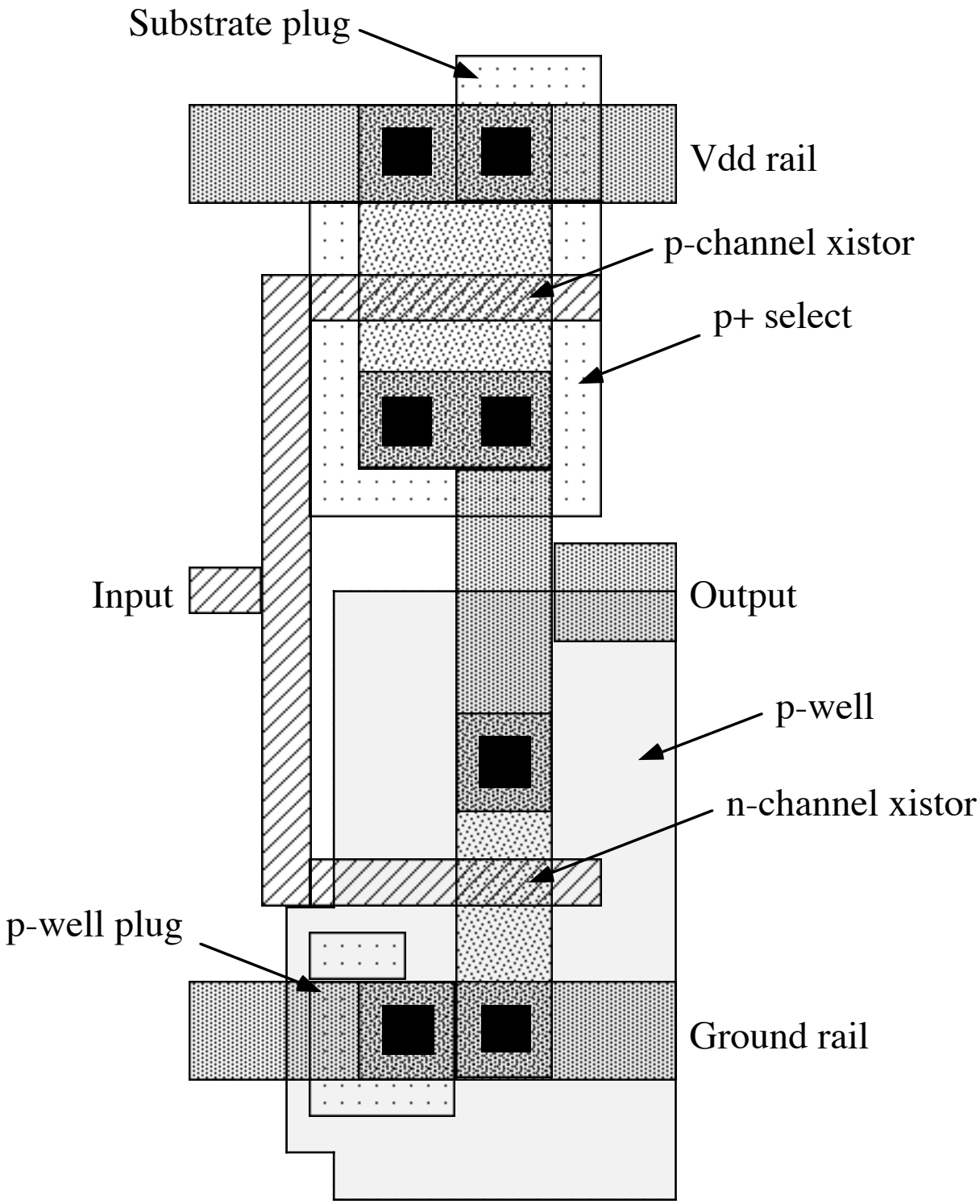


- Metal 2 is required under overglass
- Minimum size bonding pad is 100 by 100 microns
- Probe pad is 75 by 75 microns
- Overglass indicates position and size of hole in the overglass layer

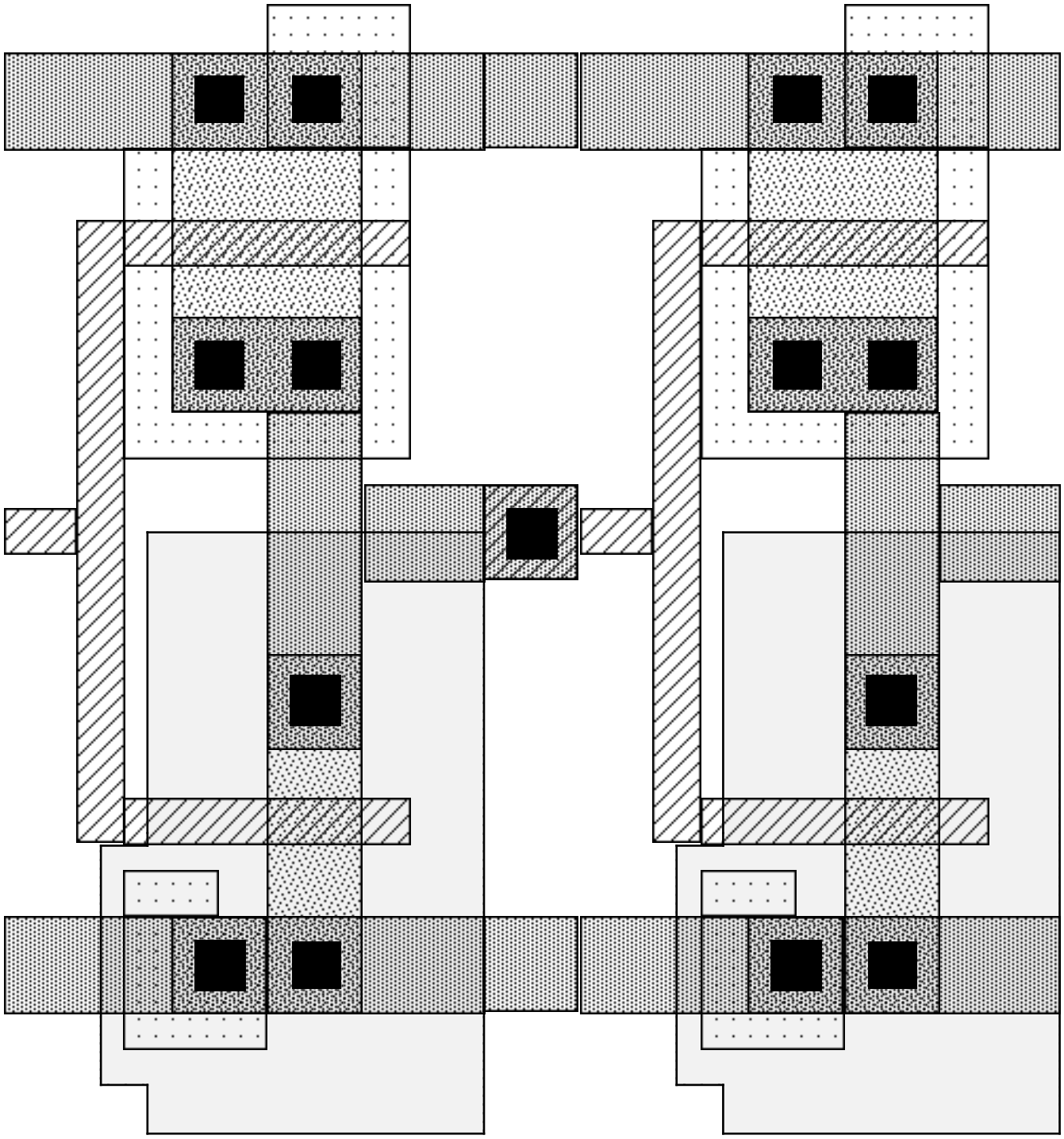
CMOS transistors (p-well process)



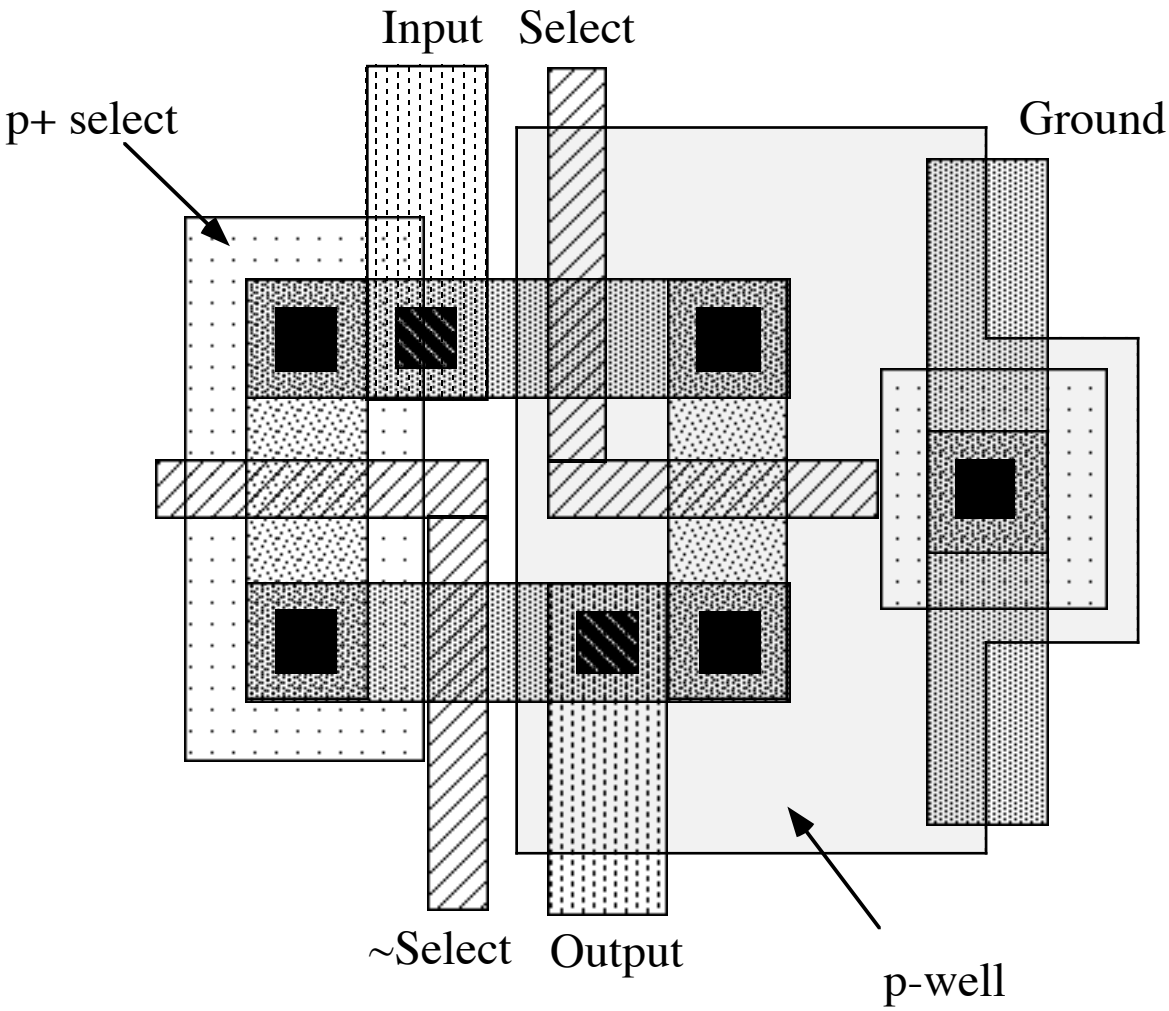
CMOS inverter (p-well process)



CMOS inverter pair



CMOS transmission gate



Resistance

- Resist the flow of current
- Used as a current limiting device
- Ohm's law

$$V = I \times R$$

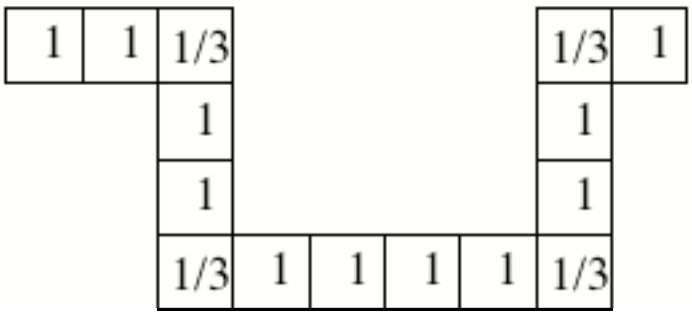
V is voltage, I is current, R is resistance

- Resistance

$$R = \frac{\rho}{t}\frac{L}{W}$$

ρ is resistivity, t is thickness, L is length, W is width

- Sheet resistance
  - t is given for a particular fabrication process
  - Resistance is stated as ohms per square
  - Estimation
    - Break shape into squares
    - Count number of squares of material
    - Multiply by material constant
    - Corners count as $1/3$ of a square



Resistance (2)

- Typical sheet resistances

Metal	0.5 Ohms / square
Silicides	3 Ohms / square
Diffusion	25 Ohms / square
Polysilicon	50 Ohms / square

- Routing priority
  - Ground rail
  - Clock lines and time critical signals
  - Positive power rail (Vdd)
- Rules of thumb
  - Route power and ground on metal
  - Route signals on metal if possible
  - Polysilicon and diffusion over short distances
  - Use metal for long distances
  - Keep wires short
  - Plan ahead for shortest wire routing
- Crossovers
  - May be necessary to route under metal
  - Use contacts to change layers
  - Metal may cross poly, n-diffusion or p-diffusion
  - Favor polysilicon for signal lines
  - Use diffusion for power connections

Capacitance

- Charge storage
- Wires and gates are all capacitors
- Charge on a capacitor

$$Q = C \times V$$

Q is charge, C is capacitance, V is voltage

- Capacitance

$$C = \frac{KA}{d}$$

K is dielectric constant, A is plate area, d is distance

- d and K are given for a particular process
- Capacitance is stated as farads per square-micron
- Precise estimation should account for
  - Area exposed to bulk
  - Side wall exposed to field
  - Side wall exposed to gate region
- Compute area and multiply by material constant
- Typical capacitances by material

Gate	4.5×10^{-4}	pF / μm^2
Polysilicon over field	0.5×10^{-4}	
n-diffusion (active)	0.9×10^{-4}	
p-diffusion (active)	0.9×10^{-4}	
Metal 1 over field	0.2×10^{-4}	
Metal 2 over field	0.1×10^{-4}	

- Keep wires short and route on metal if possible
- Use diffusion and poly for short local wires only
- Propagation depends upon the RC time constant