VLSI design

Irsim simulation

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irsim summary

- Event-driven, logic-level simulator for MOS
- Simulation models
  - Switch
    - ◊ Transistors as voltage-controlled switches
    - ◊ Use to test functionality
  - Linear (default)
    - ◊ Resistor in series with voltage-controlled switch
    - ◊ Each node has capacitance

usage

- Basic

```
irsim scmos2um.prm file.sim
```

`scmos2um.prm` - 2 micron CMOS parameters
`file.sim` - CMOS transistor network

- Setting `CAD_HOME`

```
setenv CAD_HOME /usr/local/cad
```

- Aliasing `irsim`

```
alias irsim irsim scmos2um.prm
```

- Invoking irsim with a command file

```
irsim file.sim -file.test
```

`file.sim` - CMOS transistor network
`file.test` - command file

irsim netlist format

- Technology definition

```
| units: s tech: t
```

`s` - scale linear dimensions by `s` to centimicrons
`t` - name of circuit technology

Must be first line in file if present

- p-channel transistor

```
p g s d l w
```

`g` - gate node
`s` - source node
`d` - drain node
`l` - transistor length (centimicrons)
`w` - transistor width (centimicrons)

- n-channel transistor

```
n g s d l w
```

See parameters to p-channel transistor above

- Capacitor

```
C n1 n2 value
```

`n1` - first node
`n2` - second node
`value` - capacitance in femtofarads

irsim basic commands

- Comments

```
| anything you want to say
```

- Watch one or more nodes

```
w n1 n2 ...
```

`n1` - first node
`n2` - second node, etc.

- Set one or more nodes low

```
l n1 n2 ...
```

- Set one or more nodes high

```
h n1 n2 ...
```

- Perform a single simulation step

```
s
```

- Execute commands from command file

```
@ file.test
```

- Quit and return to the Unix™ shell

```
q
```

irsim analyzer display tool

- Provides graphical waveform display
- Displays both nodes and vectors
- Additional functions through pull-down menus
  - Scroll forward and backward in time
  - Change time scale
  - Writes a PostScript file which can be printed
- Operates under X-windows only

- Display one or more nodes in waveform window

```
analyzer n1 n2 ...
```

`n1` - first node
`n2` - second node, etc.

Creates waveform window if one does not yet exist

- Abbreviated `analyzer` command

```
ana n1 n2 ...
```

- Remove all nodes and vectors from waveform display

```
clear
```

- Set which display to connect to (optional)

```
Xdisplay [host:display]
```

Beyond the basic commands

- Define a bit vector to handle a bus

```
vector name n1 n2 ...
```

`name` - vector name
`n1, n2, ...` - nodes in the vector

  - irsim supports iteration over a range of nodes
  - For example, `bus{0:3}` is equivalent to the node list: `bus0 bus1 bus2 bus3`
  - Example: `vector BUS B{7:0}`

- Assign a value to a vector

```
set name value
```

`name` - vector name
`value` - value to be assigned to vector

  - Corresponding values are assigned bit-by-bit
  - Bit values: `0`, `l`, `L`, `1`, `h`, `H`, `x` or `X`
  - Example: `set BUS 01XX1011`

- Display critical path for last transition of node(s)

```
path n1 n2 ...
```

  - Traces forward from inputs to node
  - Each transition on path has:
    - Name of the node that changed
    - New node value
    - Time of the transition
    - Delay through node since last transition

Path example

- irsim netlist for inverter pair

```
| units: 100 tech: scmos
| Inverter pair

n in in_bar GND 2 2
p in Vdd in_bar 2 4

n in_bar out GND 2 2
p in_bar Vdd out 2 4
```

- Commands

```
w out in_bar in
l in
s
h in
s
path out
```

- Execution transcript

```
58 > script pair.script
Script started on Thu Aug 15 14:41:59 1991
16 > irsim pair.sim
*** IRSIM version 8.6 ***
5 nodes; transistors: n-channel=2 p-channel
parallel txtors:none
irsim> w out in_bar in
irsim> l in
irsim> s
in=0 in_bar=1 out=0
time = 100.0ns
irsim> h in
irsim> s
in=1 in_bar=0 out=1
time = 200.0ns
irsim> path out
critical path for last transition of out:
  in -> 1 @ 100.0ns , node was an input
    in_bar -> 0 @ 100.1ns    (0.1ns)
   out -> 1 @ 100.2ns    (0.1ns)
   irsim> q
   17 > ^D
script done on Thu Aug 15 14:42:30 1991
```

Clocks and vectors

- Define a clock vector

  `clock name values`

  `name` - clock node name
  `values` - sequence of 0's and 1's

  - Node will run through sequence each cycle
  - Can define more than one `clock` for a multi-phase clock (e.g., `PHI1` and `PHI2`)

- Define vector of inputs for a node

  `V node values`

  `values` - sequence of 0's and 1's

  - After cycle, set node to next value in sequence

- Run simulator through (`n`) cycles

  `R n`

  - Run as long as longest sequence if `n` is missing
  - Start over at beginning of node sequences

- Cycle (`n` times) through clock

  `c n`

- Step the clock through one phase (simulation step)

  `p`

Clock example

- Master - slave D-latch
- Data input - `D`
- Clock input - `Clock`
- Data outputs - `Q` and `QBar`

```
37 > script mslatch.script
Script started on Thu Aug 15 15:00:19 1991
16 > irsim mslatch.1bit
*** IRSIM version 8.6 ***
18 nodes; transistors: n-channel=12 p-channel=
parallel txtors:none
irsim> clock Clock 0 1 1 0
irsim> w QBar Q D Clock
irsim> V D 0 1 0 1
irsim> R
Clock=0 D=0 Q=0 QBar=1
time = 400.0ns
Clock=0 D=0 Q=0 QBar=1
time = 400.0ns
Clock=0 D=1 Q=1 QBar=0
time = 800.0ns
Clock=0 D=1 Q=1 QBar=0
time = 800.0ns
Clock=0 D=0 Q=0 QBar=1
time = 1200.0ns
Clock=0 D=0 Q=0 QBar=1
time = 1200.0ns
Clock=0 D=1 Q=1 QBar=0
time = 1600.0ns
Clock=0 D=1 Q=1 QBar=0
time = 1600.0ns
irsim> q
17 > ^D
script done on Thu Aug 15 15:01:20 1991
38 >
```