

irsim example: Content addressable memory cell

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| Content addressable memory cell
| Weste and Eshraghian pg. 351

| Two cross-coupled inverters to form latch

n D DBar GND
p D Vdd DBar

n DBar D GND
p DBar Vdd D

| Pass transistors to Bit/~Bit data bus

n Word D Bit
n Word DBar BitBar

| Transistors for match operation

n D Bit X
n DBar BitBar X
n X Match GND

| Transistors for precharge operation

p Precharge Vdd Bit
p Precharge Vdd BitBar
p Precharge Vdd Match
```

CAM cell: irsim test commands

| Signals to watch

w Match BitBar Bit Precharge Word

| Write and read a 1

h Precharge

h Bit

l BitBar

h Word

s

x Bit BitBar

l Word

l Precharge

s

h Precharge

h Word

s

l Word

s

| Write and read a 0

h Precharge

l Bit

h BitBar

h Word

s

x Bit BitBar

l Word

l Precharge

s

h Precharge

h Word

s

l Word

s

CAM cell: irsim test commands (2)

| Do not match zero (pattern data = 1)

h Precharge

l Bit

h BitBar

s

l Precharge

s

h Precharge

s

| Match a zero (pattern data = 0)

h Precharge

h Bit

l BitBar

s

l Precharge

s

h Precharge

s

CAM cell: irsim test run

```
17 > irsim cam
*** IRSIM version 8.6 ***
10 nodes; transistors: n-channel=7 p-channel=5
parallel txtors:none
irsim> @ cam.test
Word=1 Precharge=1 Bit=1 BitBar=0 Match=0
time = 100.0ns
Word=0 Precharge=0 Bit=1 BitBar=1 Match=0
time = 200.0ns
Word=1 Precharge=1 Bit=1 BitBar=0 Match=0
time = 300.0ns
Word=0 Precharge=1 Bit=1 BitBar=0 Match=0
time = 400.0ns
Word=1 Precharge=1 Bit=0 BitBar=1 Match=0
time = 500.0ns
Word=0 Precharge=0 Bit=1 BitBar=1 Match=0
time = 600.0ns
Word=1 Precharge=1 Bit=0 BitBar=1 Match=0
time = 700.0ns
Word=0 Precharge=1 Bit=0 BitBar=1 Match=0
time = 800.0ns
Word=0 Precharge=1 Bit=0 BitBar=1 Match=0
time = 900.0ns
Word=0 Precharge=0 Bit=0 BitBar=1 Match=0
time = 1000.0ns
Word=0 Precharge=1 Bit=0 BitBar=1 Match=0
time = 1100.0ns
Word=0 Precharge=1 Bit=1 BitBar=0 Match=0
time = 1200.0ns
Word=0 Precharge=0 Bit=1 BitBar=0 Match=1
time = 1300.0ns
Word=0 Precharge=1 Bit=1 BitBar=0 Match=1
time = 1400.0ns
irsim> q
18 >
```