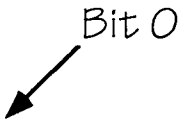
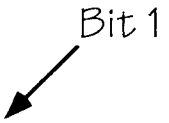
irsim example: Master / slave D-latch

```
| Instance `L' of component `MSLatch'

p Clock Vdd L_MSLatch_CB0 2 6
n Clock GND L_MSLatch_CB0 2 2
p L_MSLatch_CB0 Vdd L_MSLatch_Cx0 2 6
n L_MSLatch_CB0 GND L_MSLatch_Cx0 2 2
p D0 Vdd L_MSLatch_1N0 2 4
p L_MSLatch_CB0 L_MSLatch_1N0 L_MSLatch_2N0 2 4
n D0 L_MSLatch_2N0 L_MSLatch_3N0 2 2
n L_MSLatch_Cx0 L_MSLatch_3N0 GND 2 2
p L_MSLatch_2N0 Vdd L_MSLatch_4N0 2 4
n L_MSLatch_2N0 GND L_MSLatch_4N0 2 2
p L_MSLatch_Cx0 Vdd L_MSLatch_5N0 2 4
p L_MSLatch_4N0 L_MSLatch_5N0 L_MSLatch_2N0 2 4
n L_MSLatch_4N0 L_MSLatch_2N0 L_MSLatch_6N0 2 2
n L_MSLatch_CB0 L_MSLatch_6N0 GND 2 2
p L_MSLatch_Cx0 Vdd L_MSLatch_7N0 2 6
p L_MSLatch_4N0 L_MSLatch_7N0 QBar0 2 6
n L_MSLatch_4N0 QBar0 L_MSLatch_8N0 2 2
n L_MSLatch_CB0 L_MSLatch_8N0 GND 2 2
p QBar0 Vdd Q0 2 8
n QBar0 GND Q0 2 4
p Q0 Vdd L_MSLatch_9N0 2 6
p L_MSLatch_CB0 L_MSLatch_9N0 QBar0 2 6
n L_MSLatch_Cx0 QBar0 L_MSLatch_10N0 2 3
n Q0 L_MSLatch_10N0 GND 2 3

p Clock Vdd L_MSLatch_CB1 2 6
n Clock GND L_MSLatch_CB1 2 2
p L_MSLatch_CB1 Vdd L_MSLatch_Cx1 2 6
n L_MSLatch_CB1 GND L_MSLatch_Cx1 2 2
p D1 Vdd L_MSLatch_1N1 2 4
p L_MSLatch_CB1 L_MSLatch_1N1 L_MSLatch_2N1 2 4
n D1 L_MSLatch_2N1 L_MSLatch_3N1 2 2
n L_MSLatch_Cx1 L_MSLatch_3N1 GND 2 2
p L_MSLatch_2N1 Vdd L_MSLatch_4N1 2 4
n L_MSLatch_2N1 GND L_MSLatch_4N1 2 2
p L_MSLatch_Cx1 Vdd L_MSLatch_5N1 2 4
p L_MSLatch_4N1 L_MSLatch_5N1 L_MSLatch_2N1 2 4
n L_MSLatch_4N1 L_MSLatch_2N1 L_MSLatch_6N1 2 2
n L_MSLatch_CB1 L_MSLatch_6N1 GND 2 2
p L_MSLatch_Cx1 Vdd L_MSLatch_7N1 2 6
p L_MSLatch_4N1 L_MSLatch_7N1 QBar1 2 6
n L_MSLatch_4N1 QBar1 L_MSLatch_8N1 2 2
n L_MSLatch_CB1 L_MSLatch_8N1 GND 2 2
p QBar1 Vdd Q1 2 8
n QBar1 GND Q1 2 4
p Q1 Vdd L_MSLatch_9N1 2 6
p L_MSLatch_CB1 L_MSLatch_9N1 QBar1 2 6
n L_MSLatch_Cx1 QBar1 L_MSLatch_10N1 2 3
n Q1 L_MSLatch_10N1 GND 2 3
```





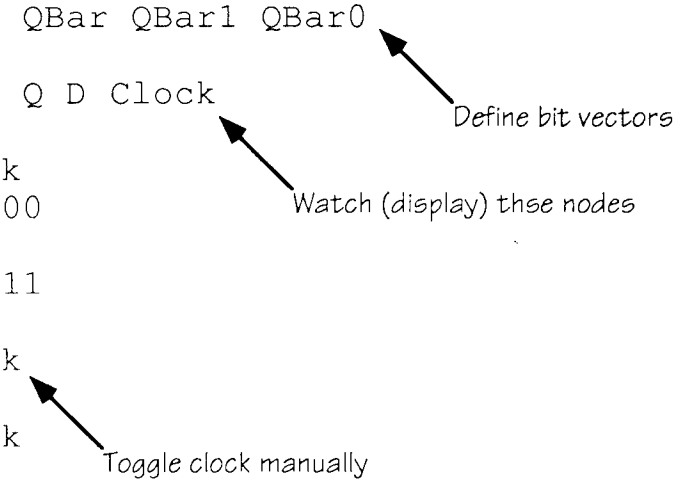
Master / slave D-latch: irsim test commands

```
| Test file for 2-bit static M/S flip/flop
| Inputs are named: Clock, D
| Outputs are named: Q QBar

vector D D1 D0
vector Q Q1 Q0
vector QBar QBar1 QBar0

w QBar Q D Clock

l Clock
set D 00
s
set D 11
s
h Clock
s
l Clock
s
set D 00
s
h Clock
s
l Clock
s
set D 11
s
h Clock
s
l Clock
s
set D 00
s
h Clock
s
l Clock
s
```



Master / slave D-latch: irsim test run

```
Script started on Wed Aug 14 10:11:17 1991
16 > irsim mslatch.2bit
*** IRSIM version 8.6 ***
33 nodes; transistors: n-channel=24 p-channel=24
parallel txtors:none
irsim> @ mslatch.test
D=00 Q=XX QBar=XX Clock=0
time = 100.0ns
D=11 Q=XX QBar=XX Clock=0
time = 200.0ns
D=11 Q=XX QBar=XX Clock=1
time = 300.0ns
D=11 Q=11 QBar=00 Clock=0
time = 400.0ns
D=00 Q=11 QBar=00 Clock=0
time = 500.0ns
D=00 Q=11 QBar=00 Clock=1
time = 600.0ns
D=00 Q=00 QBar=11 Clock=0
time = 700.0ns
D=11 Q=00 QBar=11 Clock=0
time = 800.0ns
D=11 Q=00 QBar=11 Clock=1
time = 900.0ns
D=11 Q=11 QBar=00 Clock=0
time = 1000.0ns
D=00 Q=11 QBar=00 Clock=0
time = 1100.0ns
D=00 Q=11 QBar=00 Clock=1
time = 1200.0ns
D=00 Q=00 QBar=11 Clock=0
time = 1300.0ns
irsim> q
17 >
```