irsim example: T-gate 2 to 1 mux

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| CMOS 2 to 1 multiplexer

| Author:  Paul J. Drongowski
| Address: Computer Engineering & Science
|    Case Western Reserve Univesity
|    Cleveland, Ohio 44106
| Date:    6 June 1989

| 2 to 1 multiplexer using two transmission gates
| and an inverter for selection
| Nodes:
|   A Input (data)
|   B Input (data)
|   S Input Selection input (control)
|   Out Output Selected data
| Combinational circuit where Out = (S == 0 ? A : B)

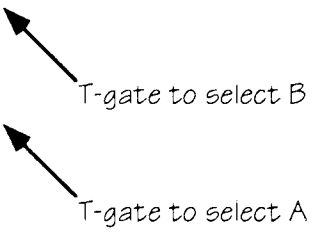
| Inverter to form complement of selection signal

n S SBar GND
p S Vdd  SBar

| Transmission gates from two inputs to one output

n S    B Output
p SBar B Output

n SBar A Output
p S    A Output
```



T-gate 2 to 1 mux: irsim test run

```
16 > irsim mux2
*** IRSIM version 8.6 ***
7 nodes; transistors: n-channel=3 p-channel=3
parallel txtors:none
irsim> w Output B A S
irsim> l A B S
irsim> s
S=0 A=0 B=0 Output=0
time = 100.0ns
irsim> h B
irsim> s
S=0 A=0 B=1 Output=0
time = 200.0ns
irsim> l B
irsim> s
S=0 A=0 B=0 Output=0
time = 300.0ns
irsim> h A
irsim> s
S=0 A=1 B=0 Output=1
time = 400.0ns
irsim> l A
irsim> s
S=0 A=0 B=0 Output=0
time = 500.0ns
irsim> h S B
irsim> s
S=1 A=0 B=1 Output=1
time = 600.0ns
irsim> l B
irsim> s
S=1 A=0 B=0 Output=0
time = 700.0ns
irsim> q
```