VLSI design

CMOS fabrication process

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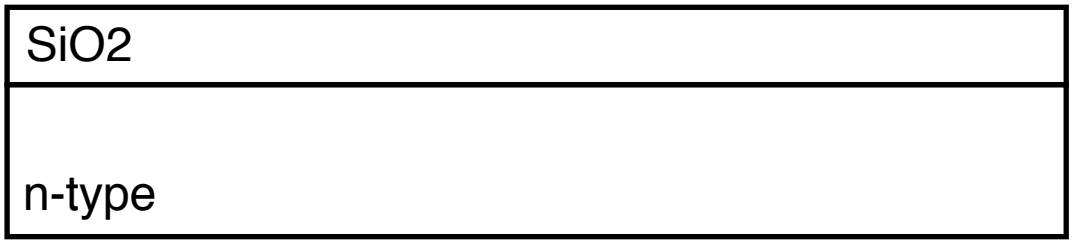
Fabrication process

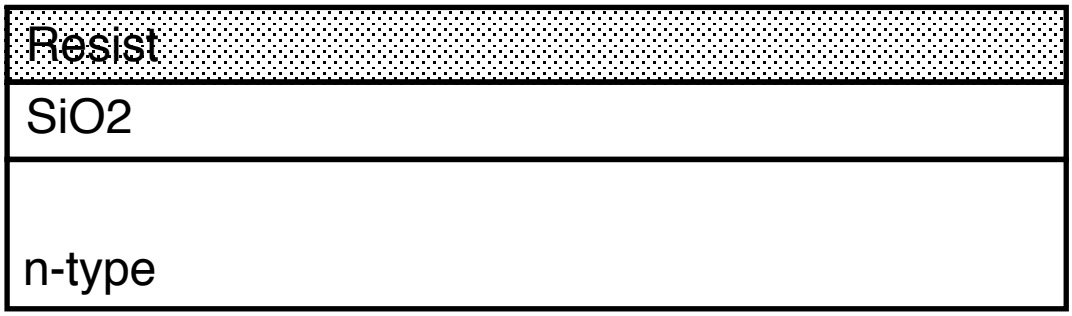
- Bits to image
  - Add alignment marks and test devices
  - Translate layout geometry to pattern generator tapes
  - Produce glass reticle
  - Reticle image is typically ten times (10X) final size
- Reticle to master masks
  - Step and repeat to obtain master masks
  - Reduce from 10X to actual size (1X)
  - Pack as many chips on wafer as possible
- Master masks to fabrication
  - Print 1X submasters
  - Save master masks for safekeeping
  - Print working masks for the fabrication line
- Perform photo / processing steps
  - Masks control placement and removal of material
  - Processes
    - Oxidation (growth of insulating layers)
    - Etching (selective removal of material)
    - Deposition
      - Evaporation - condensation
      - Sputtering (high energy ions dislodge; reattach)
      - Chemical vapor deposition
    - Diffusion
    - Ion implantation
- Separation
  - Scribe with wafer saw
  - Separate into individual chips
- Packaging
  - Mount or bond chip to carrier or IC package
  - Wire bond (gold or aluminum 1 mil wires)
  - Send to burn-in and final electrical test

Patterning

- Begin with a bare silicon wafer
- Polished disk of silicon
- Doped for n-type (CMOS p-well process)

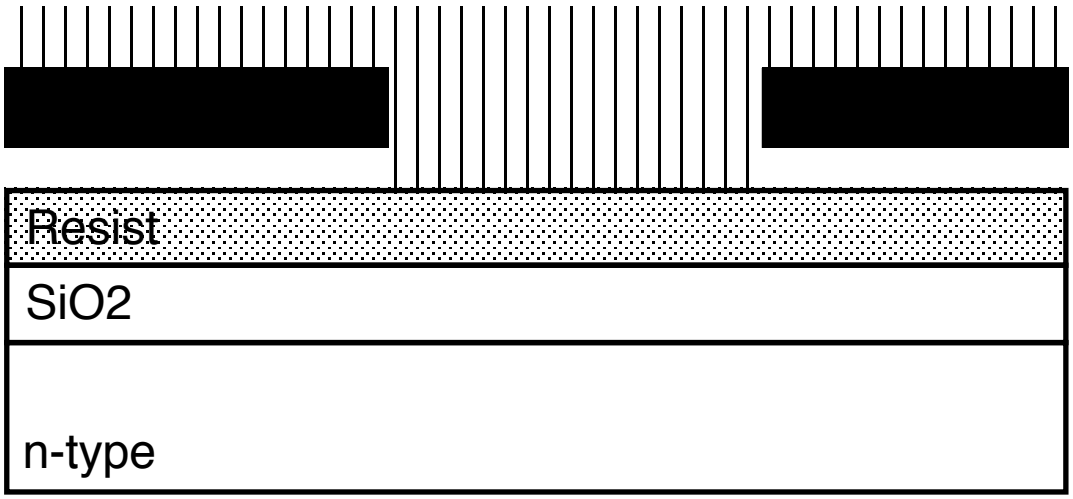


- Grow a thick layer of silicon dioxide
- Expose surface to oxygen gas at 1200 degrees C
- Layer is roughly 10000 A thick
- Will be an insulating layer

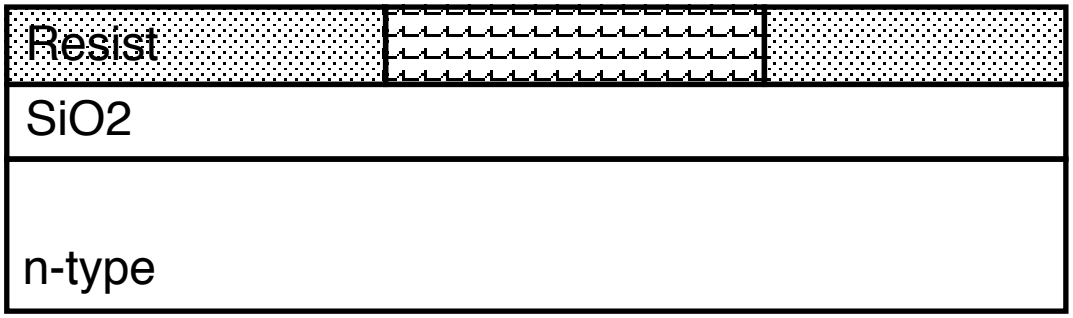


- Coat with an organic photoresist
- Resist will break down under exposure to light

Patterning (2)

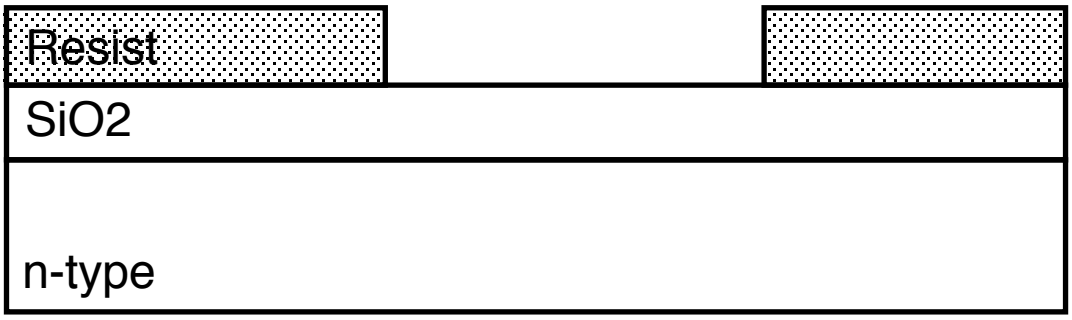


- Expose to ultraviolet (UV) light (or low energy X-rays)
- Sensitive to depth of field and wavelength
- Break down exposed portions of resist

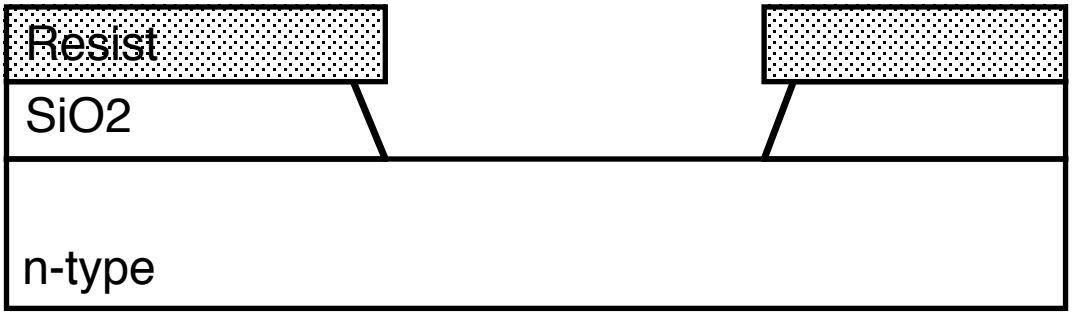


- Diffraction effects around edges of mask
- Alignment between masks
- 1 - 1.25 micron line widths (typical)

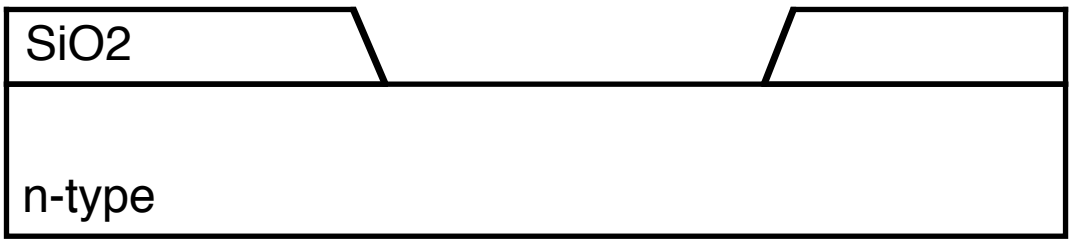
Patterning (3)



- Develop resist
- Selectively expose wafer surface

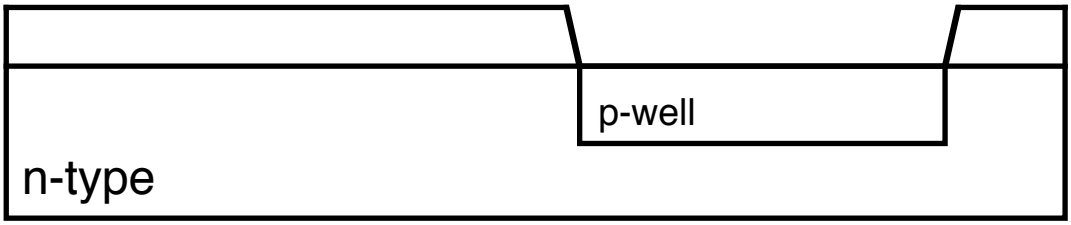


- Etch through silicon dioxide
- Attack silicon dioxide but not silicon wafer
- Selective etchant (e.g., hydrofluoric acid)

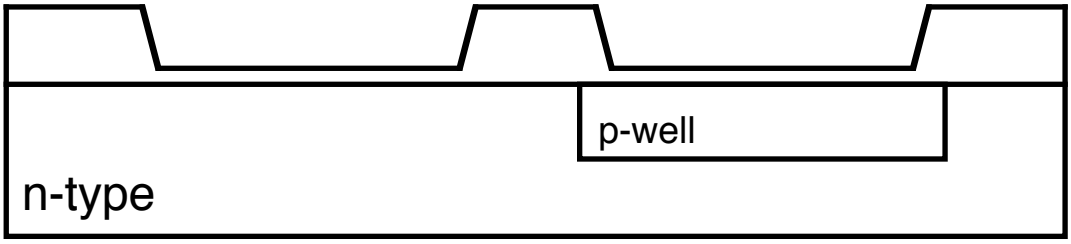


- Remove remaining resist
- Organic solvent, chromic acid or oxidize away

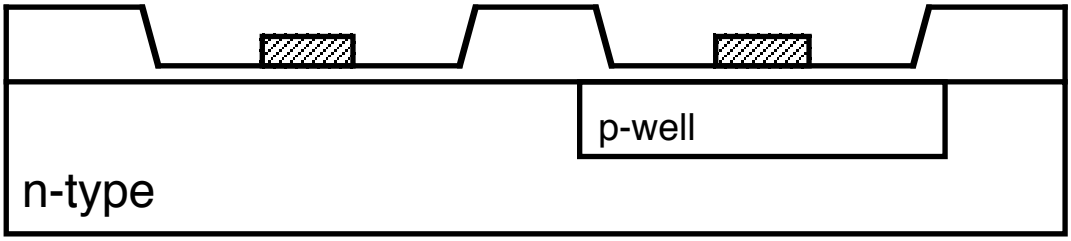
CMOS p-well process



- Mask 1 - p-well
- Deep ion diffusion (about 5 microns)
- Creates p-tub for n-channel transistors

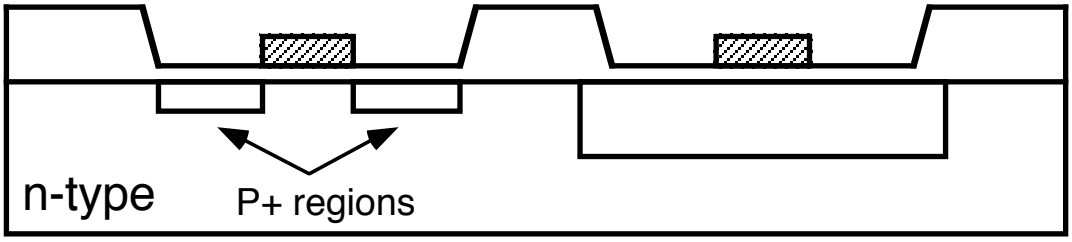


- Mask 2 - Thin oxide
- Etch thick oxide to expose p-type drain & source
- Grow thin layer of oxide (about 500 A)

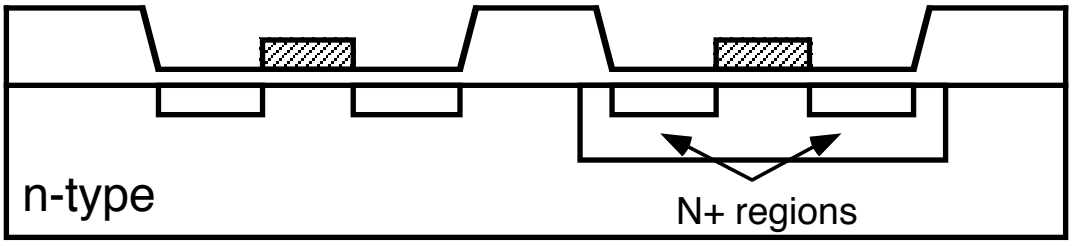


- Mask 3 - Polysilicon
- Coat with polysilicon
- Etch to obtain transistor gates and poly wires
- Gates are self-aligning

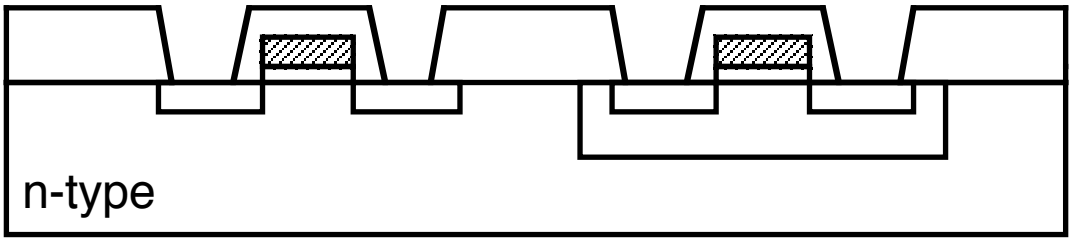
CMOS p-well process (2)



- Mask 4 - p-plus (p+ or "select" mask)
- Implant ions to form P+ regions
- Drive ions through the exposed thin oxide
- Use resist as an "ion blocker"

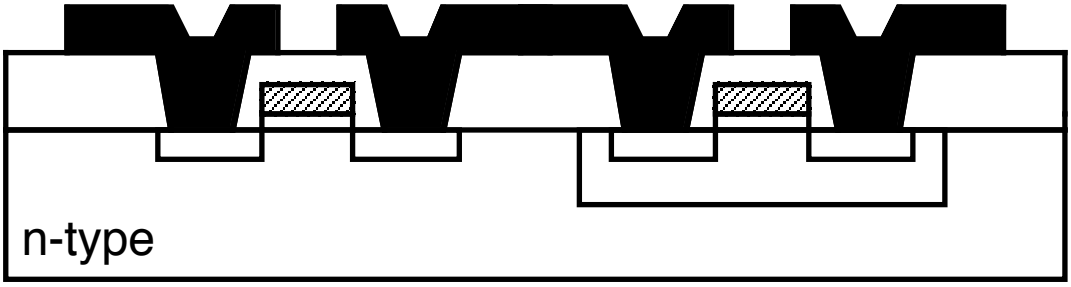


- Mask 5 - Complement of p-plus
- Form n-regions
- Diffusion or ion implantation

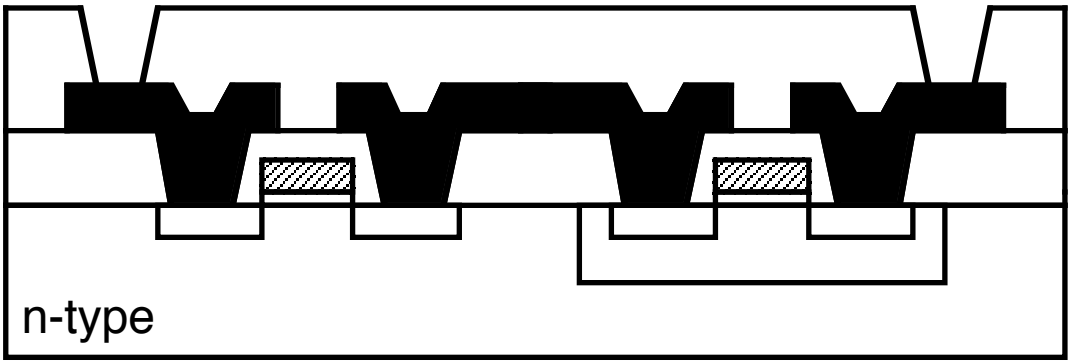


- Mask 6 - Contact cuts
- Cover with thick silicon dioxide insulator
- Etch contacts to poly, sources or drains

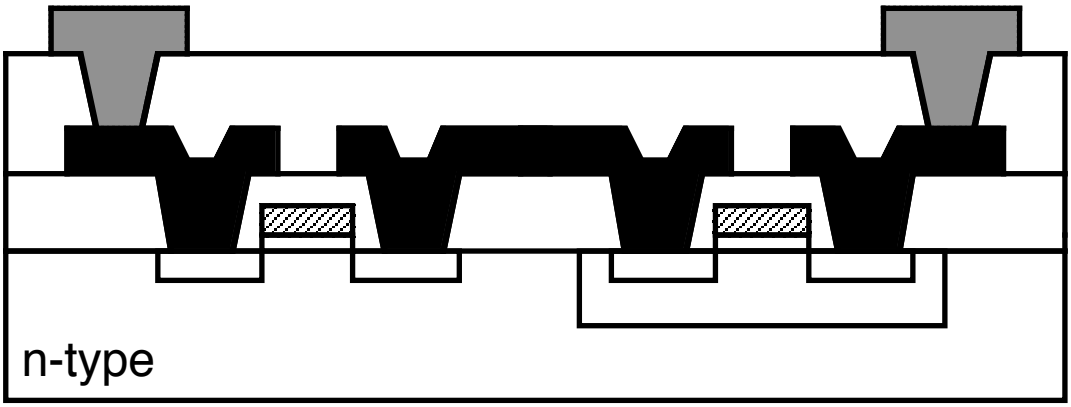
CMOS p-well process (3)



- Mask 7 - First layer of metal
- Etch for contact covers and wires



- Mask 8 - Vias (metal to metal contacts)
- Deposit thick oxide layer
- Etch contact holes



Mask 9 - Second layer of metal

Fabrication error

- Over-etching (open circuits)
- Under-etching (short circuits / bridges)
- Misalignment of masks
- Wafer distortion due to high temperature steps
- Mask distortion
  - Run out (accumulation of positioning errors)
  - Glass flatness
  - Magnification
- Focus (depth of field is about 3-5 microns)
- Differences in density of emulsion
- Differences in thickness of photoresist

Defensive design rules

- Well size, spacing and separation
  - Avoid shorts between diffusion and well
  - Ground p-well to overcome high resistance
  - Tie n-well (or n-type substrate) to Vdd
- Transistors
  - Polysilicon gate is (usually) self-aligning
  - Poly must completely cross thin oxide
- Contacts
  - Prevent open circuits due to over-etch
  - Allow metal to flow into via or contact
- Poly doping
  - Avoid p+ doping of n+ polysilicon
- Guard rings
  - Biased diffusion ring around transistor
  - Collect injected minority charge carriers
  - Prevent latch-up
- Metal thickness and separation
  - Uniform metal flow over uneven surface
  - Avoid shorts due to under-etch
  - Avoid open circuits due to over-etch or fusing