VLSI design

SPICE simulation

P.J. Drongowski
SandSoftwareSound.net

Circuit characterization

- Lateral diffusion (`LD`)
  - Reduces channel length
  - 0.25 microns (typical)

- Threshold voltage (`VTO`)
  - Varies with temperature
  - $Vt(T) = Vt(25°C) + 0.003 \times (25 - T)$
  - Vt(25°C): 0.50 (n-channel), -0.50 (p-channel)

- Intrinsic transconductance (`KP`)
  - Varies with temperature and carrier mobility
  - P-channel: 20E-5 (best), 10E-5 (worst case)
  - N-channel: 60E-5 (best), 30E-5 (worst case)

- Temperature (`.TEMP 125`)
  - Simulate over range of operating temperatures
  - 25°C (best), 95°C (nominal), 125°C (worst)

- Output loading
  - Series resistance: 0.2K ohms
  - Capacitance: 0pF (best/unloaded), 1pF (nominal)
  - Adjust according to layout measurements

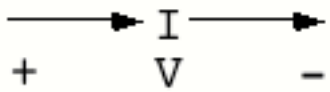
- Power supply
  - 4.2V (worst), 5.0V (nominal), 5.8V (best)

Case	Vdd	Temperature	Parameters
Worst case	4.2V	125°C	Low gain
Best case	5.8V	0°C	High gain

Table, Mehdi Hatamian, AT&T

Spice summary

- Positive current flow



- Input format
  - FORTRAN card images
  - Fields are separated by blanks, comma, equal sign or parentheses
  - Continuation convention is a "+" in column one
  - Numbers may be integers or FORTRAN floating
  - Scale factors are allowed

```
meg = 1e6
k   = 1e3
mil = 25.4e-6
m   = 1e-3
u   = 1e-6
n   = 1e-9
p   = 1e-12
f   = 1e-15
```

- Title
  - The first line in the file
  - Its contents are printed as the title on each page

- `.END` directive
  - Must be the last line in the file

- Comments
  - Comments may be placed anywhere in the file
  - A comment has an asterisk "*" in column one

Spice summary (2)

- Resistors

```
Rxxxxxxx n1 n2 value
```

`n1` node
`n2` node
`value` resistance in ohms

- Capacitors

```
Cxxxxxxx n+ n- value
```

`n+` positive node
`n-` negative node
`value` capacitance in farads

- Independent voltage sources

```
Vxxxxxxx n+ n-
```

`n+` positive node
`n-` negative node

- Power supply

```
Vxxxxxxx n+ n- DC value
```

`value` DC voltage

- By convention, node number `0` is ground
- Independent voltage sources have an infinite compliance

Spice summary (3)

- Pulse

```
Vxxxxxxx n+ n-
+ PULSE(v1 v2 td tr tf pw period)
```

`v1` initial value (volts)
`v2` pulsed (maximum) value (volts)
`td` delay time (seconds)
`tr` rise time (seconds)
`tf` fall time (seconds)
`pw` pulse width (seconds)
`period` period (seconds)

Intermediate points are determined by linear interpolation

- Piece-wise linear

```
Vxxxxxxx n+ n- PWL(t v ..... )
```

  - Each pair of values (t, v) specifies that the value of the source is v at time=t.
  - Intermediate values are determined by linear interpolation.

Spice summary (4)

- Mosfet transistors

  `Mxxxxxxx nd ng ns nb mname` *<geo-spec>*

  `nd` drain node
  `ng` gate node
  `ns` source node
  `nb` body node (usually ground)
  `mname` model name

- Geometry specification

  `l=value` channel length
  `w=value` channel width
  `ad=value` area of drain (square-microns)
  `as=value` area of drain (square-microns)
  `rd=value` drain resistance (ohms)
  `rs=value` source resistance (ohms)

- Model card

  `.MODEL mname type(` *<parameter-values>* `)`

  `mname` model name
  `type` is one of `NMOS PMOS NPN PNP D`

Spice summary (5)

- Subcircuit definition

```
.SUBCKT subname n1 <n2 n3 .... >
```

`subname` subcircuit name
`n1, ....` external nodes

  - External nodes must be numbered from one
  - Zero is reserved for ground only
  - Nodes defined in the subcircuit card are strictly local to the subcircuit

- End of subcircuit definition

```
.ENDS subname
```

`subname` subcircuit name

Ends a subcircuit definition.

- Subcircuit call

```
Xxxxxxxx n1 <n2, .... > subname
```

`subname` subcircuit name
`n1, ....` nodes

Spice summary (6)

- DC analysis

```
.DC srcname vstart vstop vincr
+ [src2 start2 stop2 incr2]
```

`srcname` name of an independent voltage source
`vstart` starting voltage
`vstop` final voltage
`vincr` increment for analysis

  - A DC analysis will be applied to the circuit
  - Specified voltage will be swept over indicated range
  - A second voltage source may be specified. The first source will be swept over each of the values of the second source
  - This kind of analysis is used to determine the transfer curve for a circuit or obtaining semiconductor device output characteristics

- Setting initial conditions

```
.NODESET v(node)=value v(node)=value ....
```

  - Helps DC analysis to find a solution
  - On the first pass, the nodes will be held to the specified voltages
  - This line may be necessary for convergence on bistable or astable circuits

```
.IC v(node)=value v(node)=value
```

  - This line sets initial transient conditions
  - It does not affect DC analysis
  - Refer to the Spice manual for additional subtleties

Spice summary (7)

- Transient analysis

  `.TRAN tstep tstop <tstart>`

  `tstep` print/plot time increment
  `tstop` time to stop transient analysis
  `tstart` time to start analysis (optional default is `0`)

  - Circuit behavior over a period of time
  - Behavior is observable through "print" and "plot"
  - If a starting time is specified, no output will be generated until simulated time achieves that value

- Printing

  `.PRINT type` *ov* <*ov ... ov*>

  `type` kind of analysis: `DC`, `TRAN`, etc.
  ov output variable (node voltage or current)
  `v(node)` voltage at a node relative to ground
  `v(n1,n2)` voltage at node n1 relative to n2
  `i(source)` current through an indep source

- Plotting

  `.PLOT type` *ov* <*ov ... ov*>

  `type` kind of analysis: `DC`, `TRAN`, etc.
  ov output variable

  - Plot the voltages (or currents)
  - There may be from 1 to 8 output variables.
  - Form of an output variable is the same as "print" except that a range of interest may be specified: `V(node)(lower,upper)`