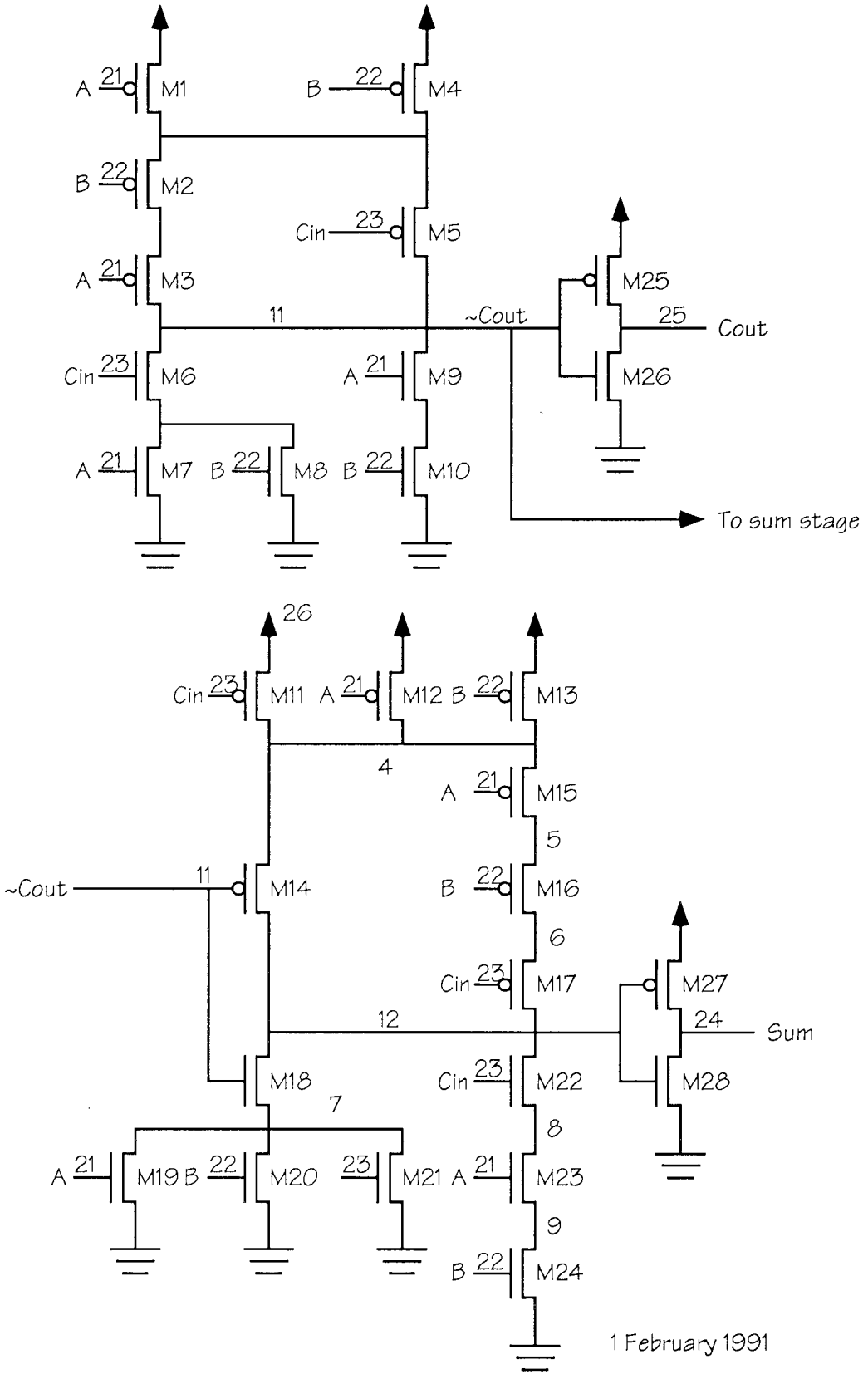
Ripple-carry adder



Spice example: Full adder

Subcircuit name and I/O nodes

Comments

Minimum size transistors

```
.SUBCKT FADDER 21 22 23 24 25 26

* Full adder - I/O node assignments
*   A    21
*   B    22
*   Cin  23
*   Sum  24
*   Cout 25
*   +5V  26
* Internal node numbers: 1:10
*  CBar = 11
*  SBar = 12

* Mx ND NG NS NB mname L=val W=val
M1   10 21 26 26 CMOSP L=2U W=4U
M2    1 22 10 26 CMOSP L=2U W=4U
M3   11 21  1 26 CMOSP L=2U W=4U
M4   10 22 26 26 CMOSP L=2U W=4U
M5   11 23 10 26 CMOSP L=2U W=4U
M6    2 23 11  0 CMOSN L=2U W=2U
M7    2 21  0  0 CMOSN L=2U W=2U
M8    2 22  0  0 CMOSN L=2U W=2U
M9    3 21 11  0 CMOSN L=2U W=2U
M10   3 22  0  0 CMOSN L=2U W=2U
M11   4 23 26 26 CMOSP L=2U W=4U
M12   4 21 26 26 CMOSP L=2U W=4U
M13   4 22 26 26 CMOSP L=2U W=4U
M14  12 11  4 26 CMOSP L=2U W=4U
M15   5 21  4 26 CMOSP L=2U W=4U
M16   6 22  5 26 CMOSP L=2U W=4U
M17  12 23  6 26 CMOSP L=2U W=4U
M18   7 11 12  0 CMOSN L=2U W=2U
M19   7 21  0  0 CMOSN L=2U W=2U
M20   7 22  0  0 CMOSN L=2U W=2U
M21   7 23  0  0 CMOSN L=2U W=2U
M22  12 23  8  0 CMOSN L=2U W=2U
M23   8 21  9  0 CMOSN L=2U W=2U
M24   9 22  0  0 CMOSN L=2U W=2U
* Invert to get Cout
M25  25 11 26 26 CMOSP L=2U W=4U
M26  25 11  0  0 CMOSN L=2U W=2U
* Invert to get Sum
M27  24 12 26 26 CMOSP L=2U W=4U
M28  24 12  0  0 CMOSN L=2U W=2U
.ENDS
```

Spice example: 16 bit ripple carry adder

```
* Node assignments
*
*   A<15:0>     - 16 to 1
*   B<15:0>     - 36 to 21
*   Cin         - 40
*   Cout<15:0>  - 56 to 41
*   Sum<15:0>   - 76 to 61

*       A     B   Cin   Sum Cout   Vdd
XADD0   1    21    40    61    41   100 FADDER
XADD1   2    22    41    62    42   100 FADDER
XADD2   3    23    42    63    43   100 FADDER
XADD3   4    24    43    64    44   100 FADDER

XADD4   5    25    44    65    45   100 FADDER
XADD5   6    26    45    66    46   100 FADDER
XADD6   7    27    46    67    47   100 FADDER
XADD7   8    28    47    68    48   100 FADDER

XADD8   9    29    48    69    49   100 FADDER
XADD9  10    30    49    70    50   100 FADDER
XADDA  11    31    50    71    51   100 FADDER
XADDB  12    32    51    72    52   100 FADDER

XADDC  13    33    52    73    53   100 FADDER
XADDD  14    34    53    74    54   100 FADDER
XADDE  15    35    54    75    55   100 FADDER
XADDF  16    36    55    76    56   100 FADDER
```

16 full adders

Instance name

Subcircuit name

16 bit ripple carry adder: Input voltage sources

```
* Inputs to full adder

VA0 1 0 PWL 0N 0V 160N 0V
VA1 2 0 PWL 0N 0V 160N 0V
VA2 3 0 PWL 0N 0V 160N 0V
VA3 4 0 PWL 0N 0V 160N 0V
VA4 5 0 PWL 0N 0V 160N 0V
VA5 6 0 PWL 0N 0V 160N 0V
VA6 7 0 PWL 0N 0V 160N 0V
VA7 8 0 PWL 0N 0V 160N 0V
VA8 9 0 PWL 0N 0V 160N 0V
VA9 10 0 PWL 0N 0V 160N 0V
VAA 11 0 PWL 0N 0V 160N 0V
VAB 12 0 PWL 0N 0V 160N 0V
VAC 13 0 PWL 0N 0V 160N 0V
VAD 14 0 PWL 0N 0V 160N 0V
VAE 15 0 PWL 0N 0V 160N 0V
VAF 16 0 PWL 0N 0V 160N 0V
VB0 21 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VB1 22 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VB2 23 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VB3 24 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VB4 25 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VB5 26 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VB6 27 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VB7 28 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VB8 29 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VB9 30 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VBA 31 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VBB 32 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VBC 33 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VBD 34 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VBE 35 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VBF 36 0 PWL 0N 0V 40N 0V 50N 5V 160N 5V
VCin 40 0 PWL 0N 0V 80N 0V 90N 5V 120N 5V
+ 130N 0V 160N 0V
```

Piecewise linear voltage source
+ node / - node
Time - voltage pairs

16 bit ripple carry adder: Loads and analysis

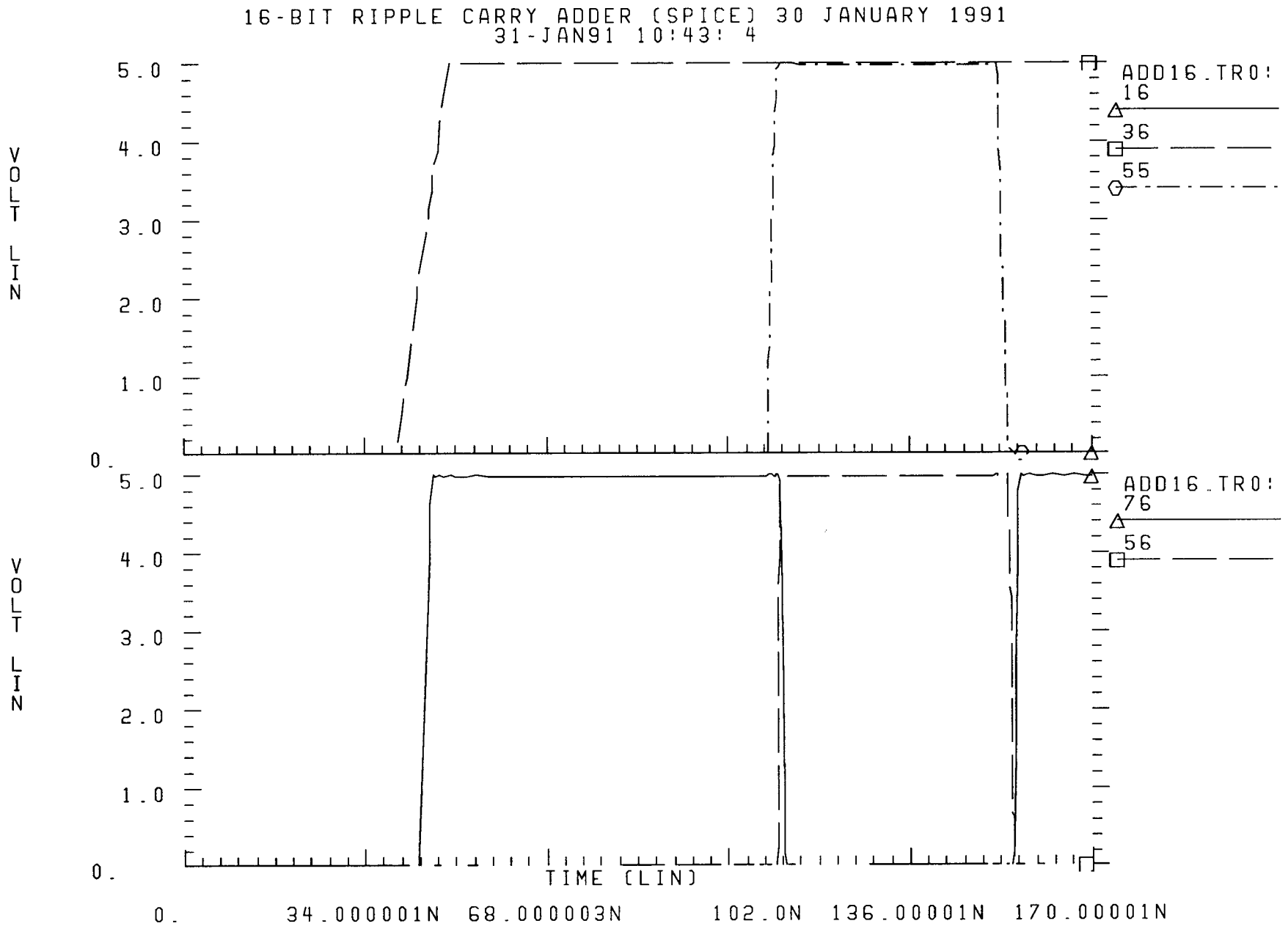
```
* Capacitive load on adder outputs
CS0 61 0 0.01P
CS1 62 0 0.01P
CS2 63 0 0.01P
CS3 64 0 0.01P
CS4 65 0 0.01P
CS5 66 0 0.01P
CS6 67 0 0.01P
CS7 68 0 0.01P
CS8 69 0 0.01P
CS9 70 0 0.01P
CSA 71 0 0.01P
CSB 72 0 0.01P
CSC 73 0 0.01P
CSD 74 0 0.01P
CSE 75 0 0.01P
CSF 76 0 0.01P

CC0 41 0 0.01P
CC1 42 0 0.01P
CC2 43 0 0.01P
CC3 44 0 0.01P
CC4 45 0 0.01P
CC5 46 0 0.01P
CC6 47 0 0.01P
CC7 48 0 0.01P
CC8 49 0 0.01P
CC9 50 0 0.01P
CCA 51 0 0.01P
CCB 52 0 0.01P
CCC 53 0 0.01P
CCD 54 0 0.01P
CCE 55 0 0.01P
CCF 56 0 0.01P

* Positive supply voltage
VDD 100 0 5V

.WIDTH OUT=80
.TRAN 1NS 210NS

*       A15   B15  Cin0 Cin15 Cout15 Sum15
.PLOT V(16) V(36) V(40) V(55)  V(56) V(76)

.END
```

Capacitor name
+ node / - node
Capacitance

Voltage source name
+ node / - node
Voltage

Transient analysis (voltage over time)
Time increment - simulation time

Node voltages to plot


16-BIT RIPPLE CARRY ADDER (SPICE) 30 JANUARY 1991
31-JAN91 10:43: 4
VOLT LIN
5.0
4.0
3.0
2.0
1.0
0.
ADD16.TR0:
16
36
55
VOLT LIN
5.0
4.0
3.0
2.0
1.0
0.
ADD16.TR0:
76
56
TIME (LIN)
0.
34.000001N
68.000003N
102.0N
136.00001N
170.00001N