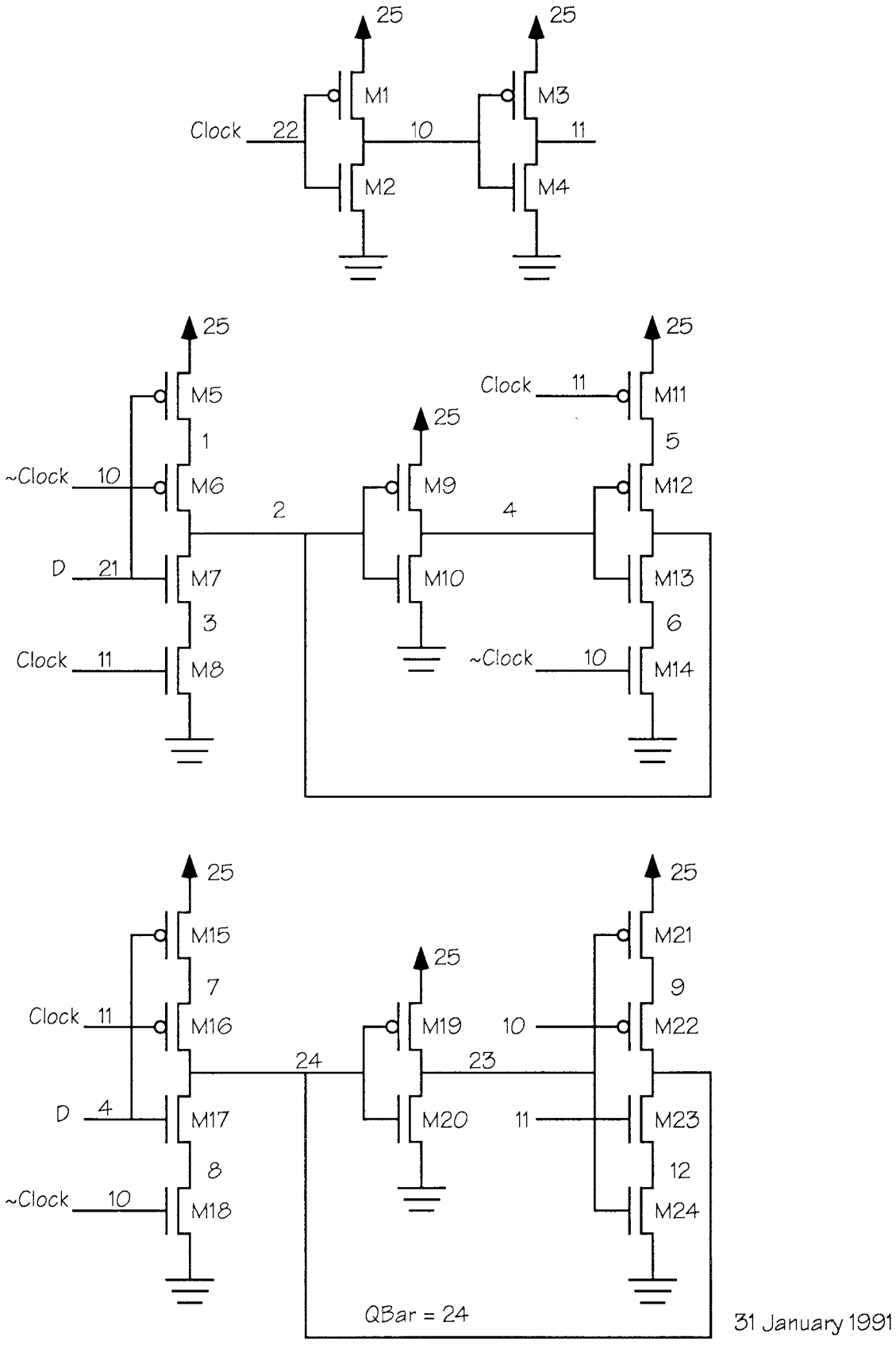
Master slave D-latch



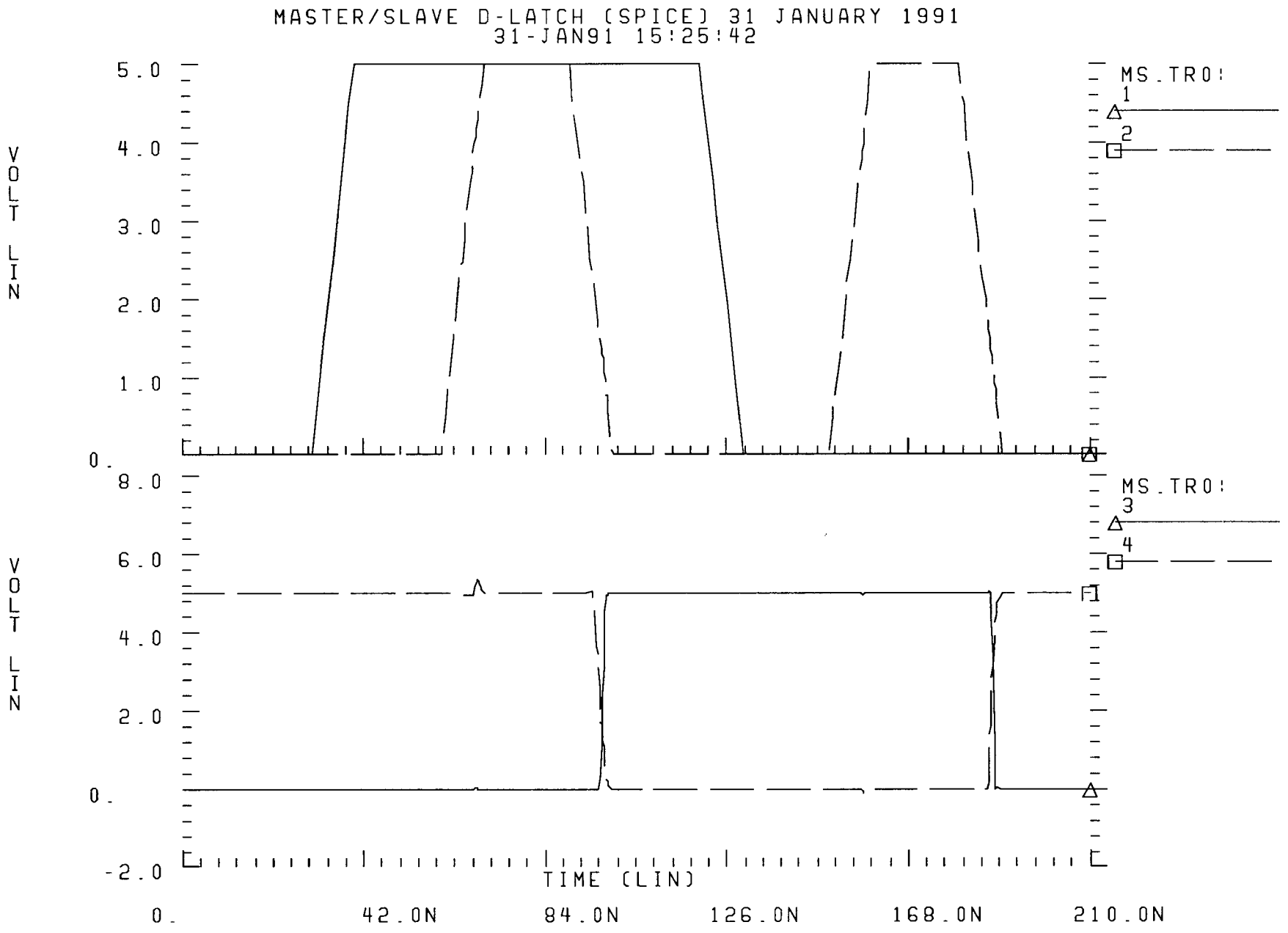
31 January 1991

Spice example: Master / slave D-latch

```
.SUBCKT MSD 21 22 23 24 25

* Master/slave D-latch - I/O node assignments
*    D      21
*    Clock  22
*    Q      23
*    QBar   24
*    +5V    25
*    Nodes  1 2 3 4 5 6 7 8 9 12
*    CB     10
*    Cx     11
*    ND NG NS NB mname L=val W=val
M1   10 22 25 25 CMOSP L=2U W=6U
M2   10 22  0  0 CMOSN L=2U W=2U
M3   11 10 25 25 CMOSP L=2U W=6U
M4   11 10  0  0 CMOSN L=2U W=2U
M5    1 21 25 25 CMOSP L=2U W=4U
M6    2 10  1 25 CMOSP L=2U W=4U
M7    3 21  2  0 CMOSN L=2U W=2U
M8    0 11  3  0 CMOSN L=2U W=2U
M9    4  2 25 25 CMOSP L=2U W=4U
M10   4  2  0  0 CMOSN L=2U W=2U
M11   5 11 25 25 CMOSP L=2U W=4U
M12   2  4  5 25 CMOSP L=2U W=4U
M13   6  4  2  0 CMOSN L=2U W=2U
M14   0 10  6  0 CMOSN L=2U W=2U
M15   7 11 25 25 CMOSP L=2U W=6U
M16 24  4  7 25 CMOSP L=2U W=6U
M17   8  4 24  0 CMOSN L=2U W=2U
M18   0 10  8  0 CMOSN L=2U W=2U
M19 23 24 25 25 CMOSP L=2U W=8U
M20 23 24  0  0 CMOSN L=2U W=4U
M21   9 23 25 25 CMOSP L=2U W=6U
M22 24 10  9 25 CMOSP L=2U W=6U
M23 12 11 24  0 CMOSN L=2U W=3U
M24  0 23 12  0 CMOSN L=2U W=3U
.ENDS
```

Master / slave D-latch: Spice test

```
XMSD 1 2 3 4 5 MSD

* Inputs to D-latch

VD 1 0 PWL 0N 0V 30N 0V 40N 5V 120N 5V 130N 0V
+ 210N 0V
VCLOCK 2 0 PWL 0N 0V 60N 0V 70N 5V 90N 5V 100N 0V
+ 150N 0V 160N 5V 180N 5V 190N 0V 210N 0V

* Capacitive load on latch outputs
CQ    3 0 0.01P
CQBAR 4 0 0.01P

* Positive supply voltage
VDD 5 0 5V

.WIDTH OUT=80
.TRAN 1NS 210NS
.PLOT V(1) V(2) V(3) V(4)

.END
```


MASTER/SLAVE D-LATCH (SPICE) 31 JANUARY 1991
31-JAN91 15:25:42
VOLT LIN
5.0
4.0
3.0
2.0
1.0
0.
MS.TR0:
1
2
VOLT LIN
8.0
6.0
4.0
2.0
0.
-2.0
MS.TR0:
3
4
TIME (LIN)
0.
42.0N
84.0N
126.0N
168.0N
210.0N

M/S D flip-flop with reset