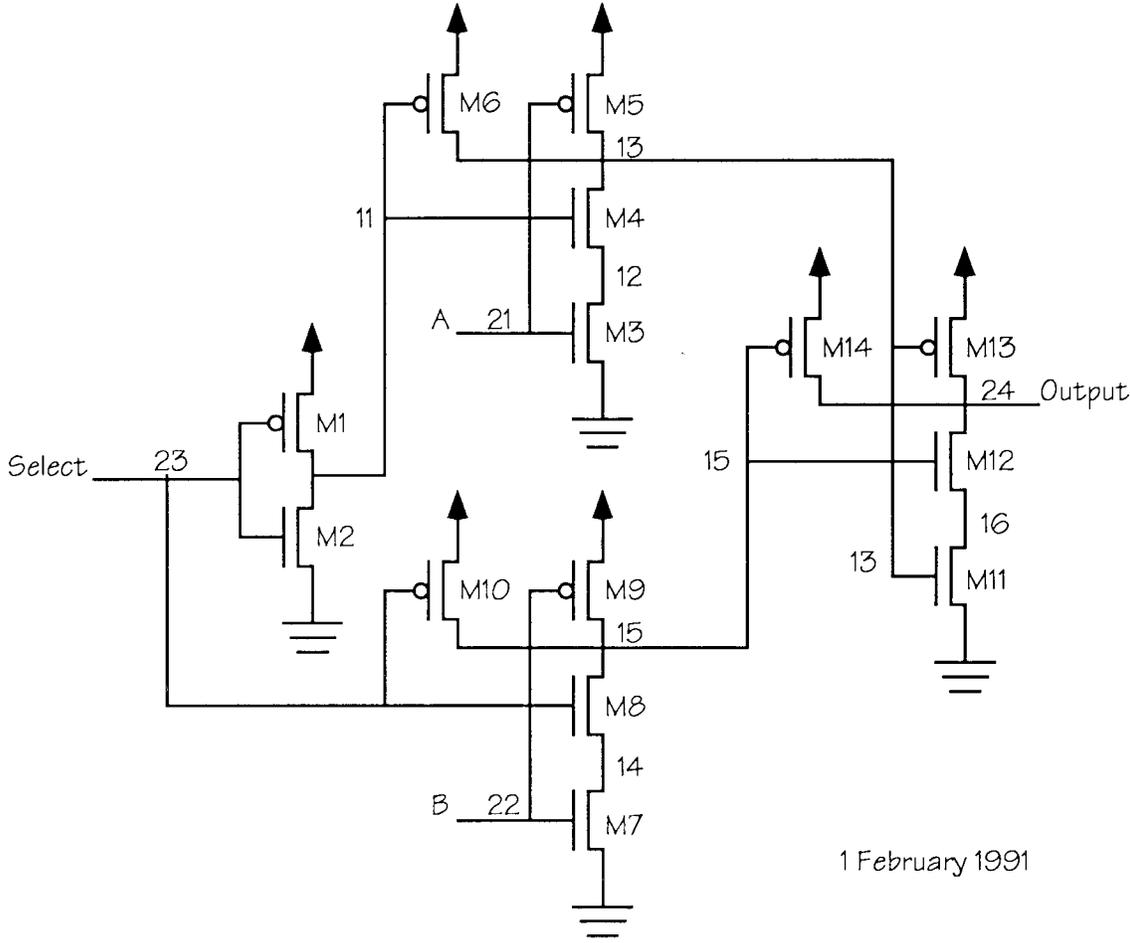


Two to one multiplexer



Spice example: Two to one multiplexer

2 to 1 multiplexer/AND-OR logic (SPICE) 31 January 1991

Options

Title line

.OPTION POST=1

Model definition and parameters

.MODEL CMOSN NMOS LEVEL=2 LD=0.250000U TOX=410.000000E-10
+ NSUB=8.358422E+15 VTO=0.816866 KP=5.883000E-05
+ GAMMA=0.6254 PHI=0.6 UO=698.5 UEXP=0.169549
+ UCRIT=27275.7 DELTA=2.33983 VMAX=68149.4 XJ=0.250000U
+ LAMBDA=2.951013E-02 NFS=3.912943E+12 NEFF=1
+ NSS=1.000000E+12 TPG=1.000000 RSH=19.400000
+ CGDO=3.158363E-10 CGSO=3.158363E-10 CGBO=5.459241E-10
+ CJ=1.400700E-04 MJ=0.782300 CJSW=7.096400E-10
+ MJSW=0.382500 PB=0.800000

Comments

* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.46 um

Threshold

Thickness

.MODEL CMOSP PMOS LEVEL=2 LD=0.250000U TOX=410.000000E-10
+ NSUB=5.613789E+15 VTO=-0.782334 KP=2.000000E-05
+ GAMMA=0.5126 PHI=0.6 UO=237.5 UEXP=0.261971 UCRIT=37097
+ DELTA=2.580969E-06 VMAX=100000 XJ=0.050000U
+ LAMBDA=3.989719E-02 NFS=1.000000E+11 NEFF=1.001
+ NSS=1.000000E+12 TPG=-1.000000 RSH=101.300000
+ CGDO=3.158363E-10 CGSO=3.158363E-10 CGBO=5.393152E-10
+ CJ=2.502200E-04 MJ=0.545500 CJSW=3.278600E-10
+ MJSW=0.325800 PB=0.800000

* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.49 um

Two to one multiplexer (2)

```

Subcircuit definition
Name
I/O nodes
Comments
.SUBCKT MUX 21 22 23 24 25

* 2 to 1 multiplexor - I/O node assignments
*   A      21
*   B      22
*   S      23
*   Z      24
*   +5V    25
*   SBar   11
*   Nodes  12 13 14 15 16

Local nodes
Transistors
*   ND NG NS NB mname L=val W=val
M1  11 23 25 25 CMOSP L=2U W=4U
M2  11 23  0  0 CMOSN L=2U W=2U
M3   0 21 12  0 CMOSN L=2U W=2U
M4  12 11 13  0 CMOSN L=2U W=2U
M5  13 21 25 25 CMOSP L=2U W=4U
M6  13 11 25 25 CMOSP L=2U W=4U
M7   0 22 14  0 CMOSN L=2U W=2U
M8  14 23 15  0 CMOSN L=2U W=2U
M9  15 22 25 25 CMOSP L=2U W=4U
M10 15 23 25 25 CMOSP L=2U W=4U
M11  0 13 16  0 CMOSN L=2U W=2U
M12 16 15 24  0 CMOSN L=2U W=2U
M13 24 13 25 25 CMOSP L=2U W=4U
M14 24 15 25 25 CMOSP L=2U W=4U
.ENDS

Subcircuit call (instance)
Output loading
XMUX  1 2 3 4 5 MUX

* Capacitive load on mux output
CZ   4 0 0.01P

Name  Nodes (+/-)  Capacitance

```

Two to one multiplexer example (3)

+ node
- node

* Inputs to full adder

Input voltage sources

```
VA 1 0 PWL 0N 0V 80N 0V 90N 5V 160N 5V 170N 0V 180N 0V
VB 2 0 PWL 0N 0V 40N 0V 50N 5V 100N 5V 110N 0V 140N 0V
+ 150N 5V 160N 5V 170N 0V 180N 0V
VC 3 0 PWL 0N 0V 20N 0V 30N 5V 60N 5V 70N 0V 120N 0V
+ 130N 5V 160N 5V 170N 0V 180N 0V
```

Time Voltage

* Positive supply voltage

```
VDD 5 0 5V
```

Transient analysis

Voltages to plot

```
.WIDTH OUT=80
.TRAN 1NS 200NS
.PLOT V(1) V(2) V(3) V(4)
.END
```

2 TO 1 MULTIPLEXOR/AND-OR LOGIC (SPICE) 31 JANUARY 1991
31-JAN91 11:31:13

