VLSI design

Introduction to nMOS circuits

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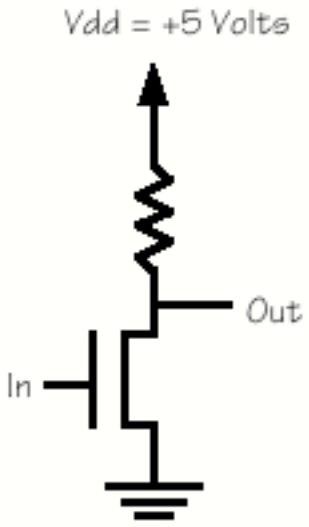
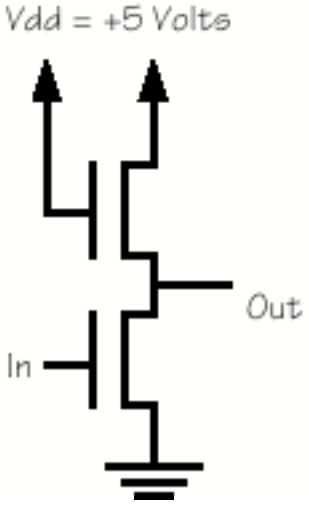
Inverter using pull-up resistor



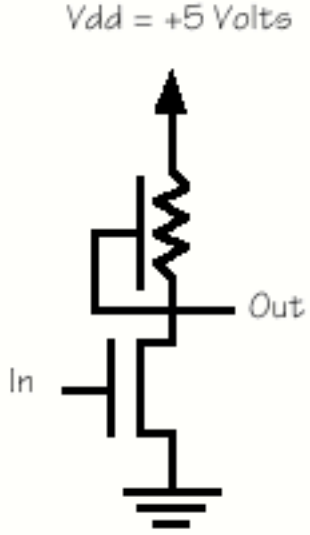
- Resistor is current limiting device
- Resistor pulls output up to 5 volts
- Switch pulls output toward ground
- Voltage divider
- Must pull output below Vth
- Poly is about 10 ohms / square
- Need 1000 squares for 10K ohms

Inverter using enhancement pull-up



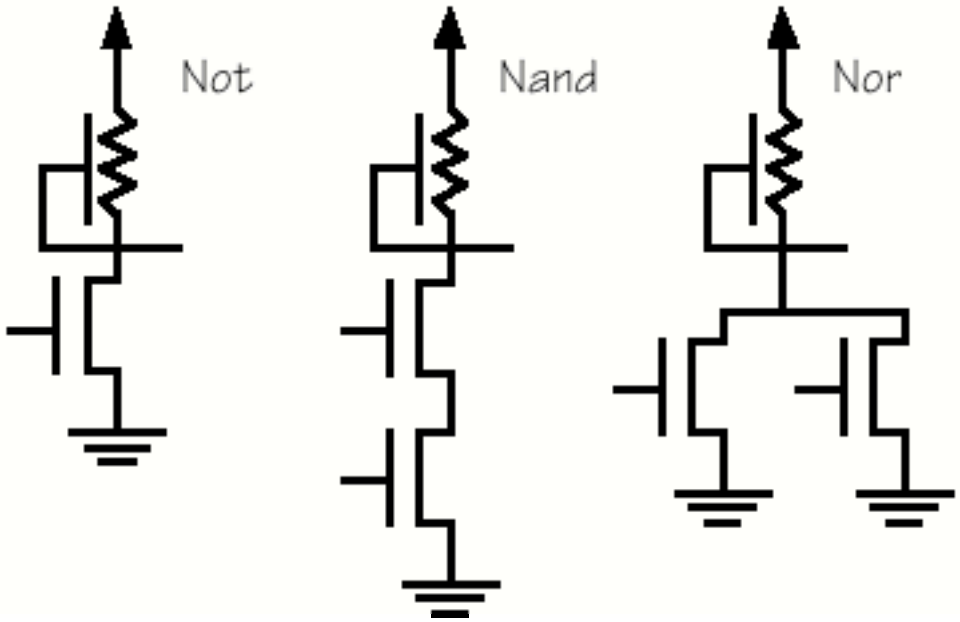
- Use high channel resistance
- Sheet resistance is 10Kohms/square
- Gives a compact pull-up resistor
- Voltage drop across channel is Vth
- Vth of 1 volt is typical in nMOS
- Output rises to only 4 volts

Inverter using depletion mode pull-up



- Dope pull-up channel
- Implant negative ions into channel
- Sets Vth to -3 volts (typical)
- Channel always is turned on
- Channel provides pull-up resistance
- Pull-up must be carefully sized
- No voltage drop across channel
- Full 5 volt output

Logic gates

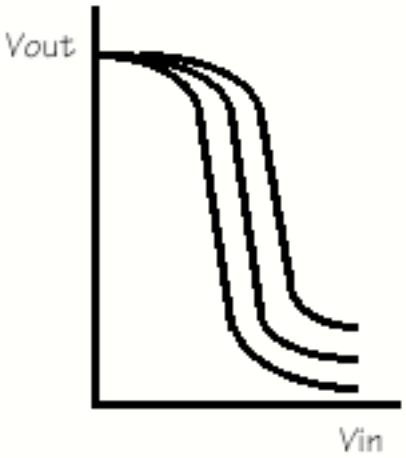


Gain

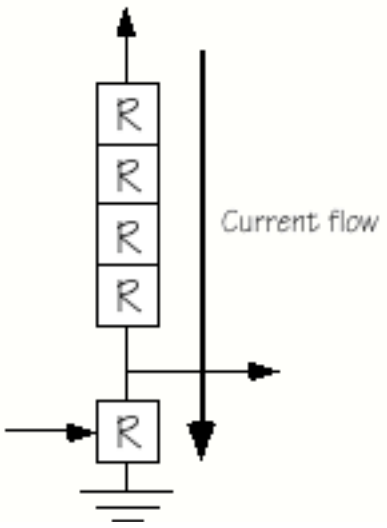
- Vout versus Vin transfer characteristics
- Gain is the slop in the middle of the curve
- Curve moves up with decreasing gain
- Curve moves down with increasing gain
- Tail of the curve must not exceed Vth (+1 volt)
- Gain is usually greater than or equal to four

- Gain = $$\frac{L_{Pull\text{-}up} / W_{Pull\text{-}up}}{L_{Pull\text{-}down} / W_{Pull\text{-}down}}$$

- Use Spice DC analysis

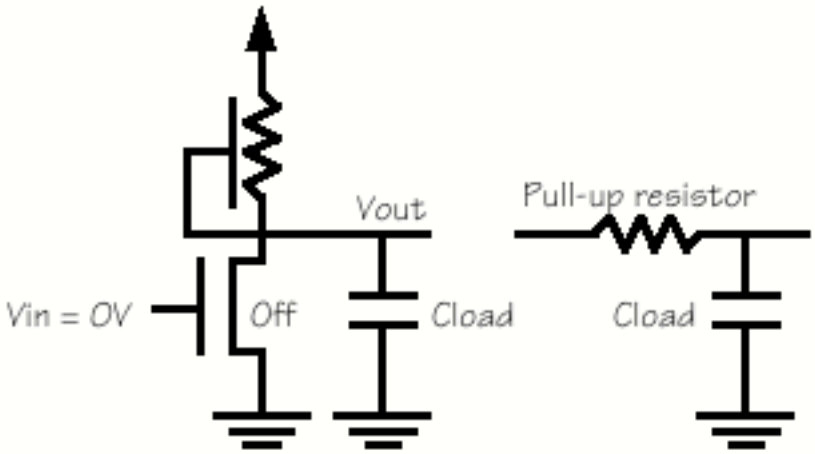


Current consumption

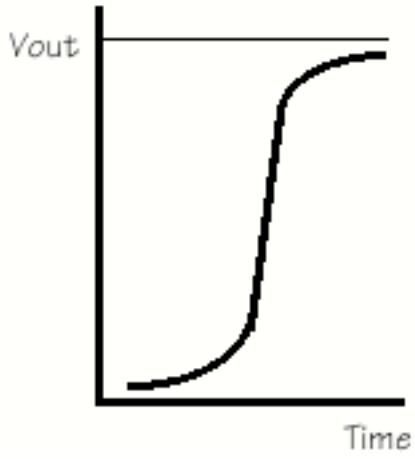


- Let R = 10K ohms
- Total resistance is 50K ohms
- Current consumption
  I = 5 volts / 50K ohms = 0.1 mA
- Power dissipation
  P = 5 volts × 0.1 mA = 0.5 mW

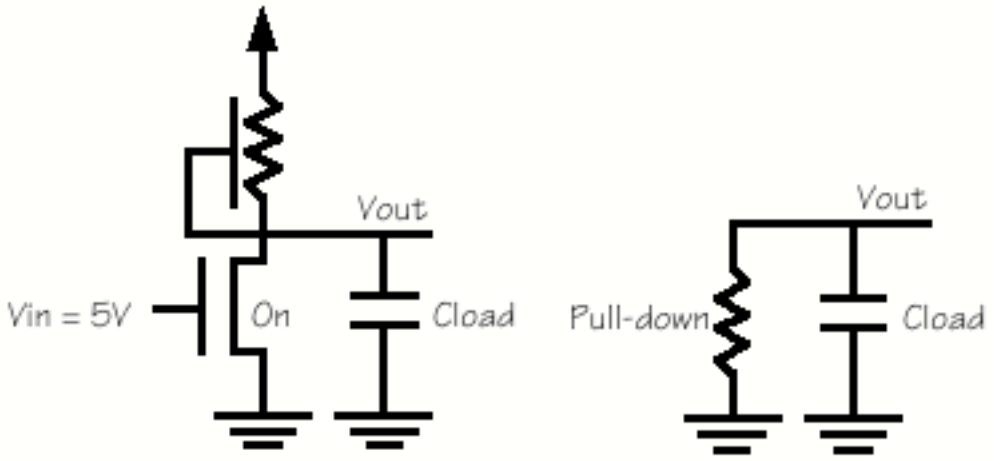
Rise time



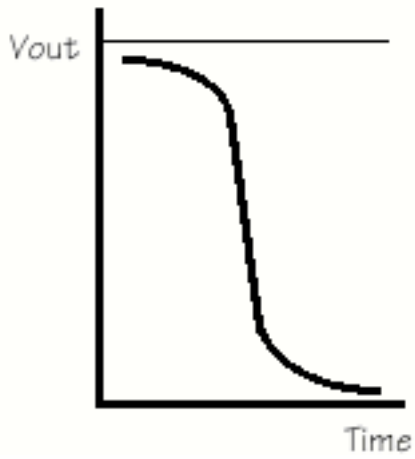
- Enhancement transistor is switched off
- $V(t) = Vdd \times (1 - e^{-t/RC})$
- $T_{rise} = K \times (\frac{L}{W}) \times C_{load}$ (nanoseconds)
  - L and W are length and width of pull-up transistor
  - K is a timing constant (typically 60)
  - C_{load} is the load capacitance in picofarads



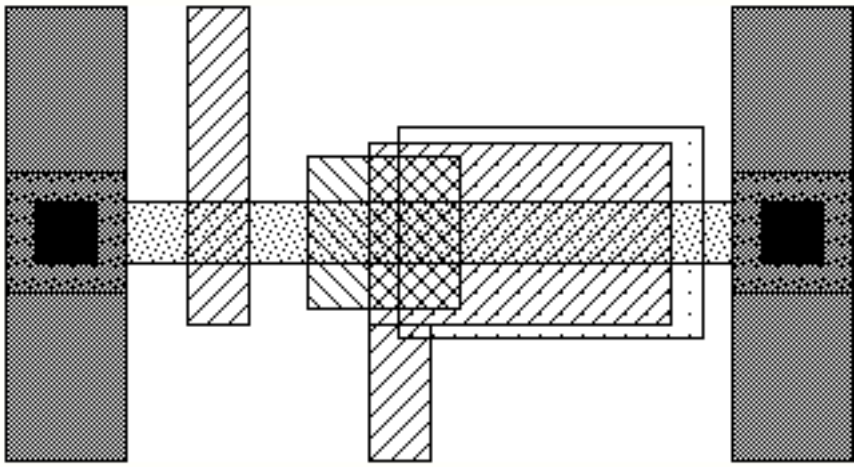
Fall time

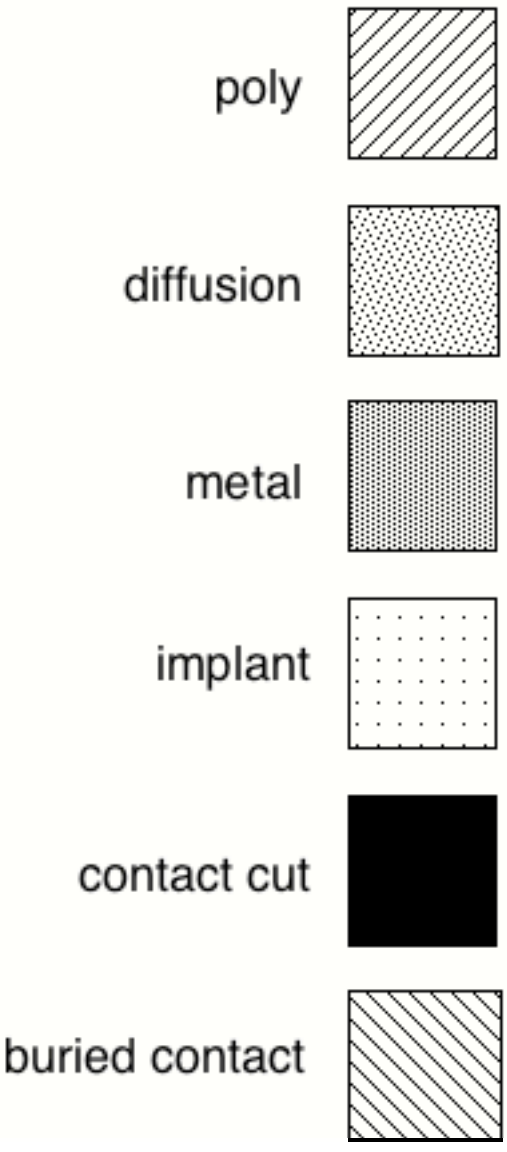


- Enhancement transistor is switched on
- Load capacitance is discharged through pull-down
- $T_{fall} = K \times (\frac{L}{W}) \times C_{load}$ (nanoseconds)
  - L and W are length and width of pull-down transistor
  - K is a timing constant (typically 27)
  - C_{load} is the load capacitance in picofarads

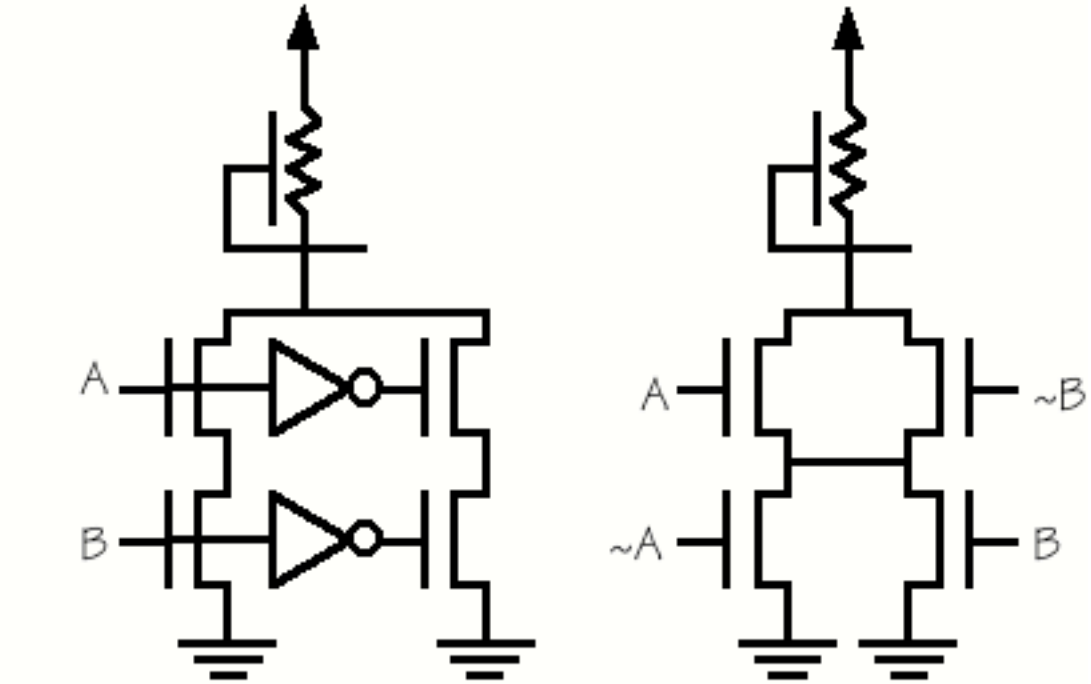


nMOS layout

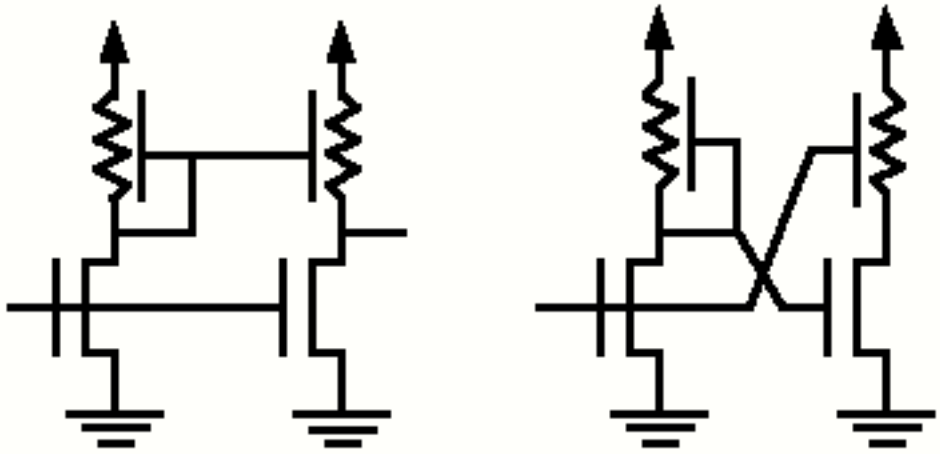




Exclusive OR



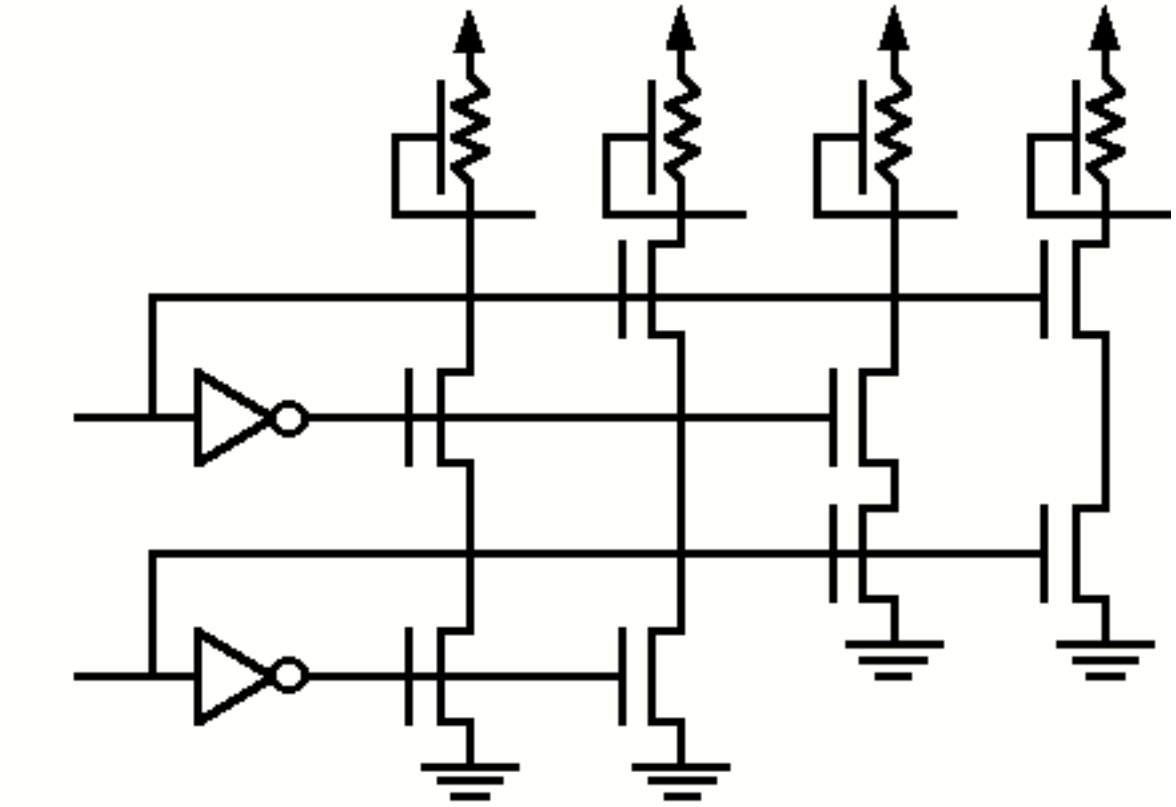
Superbuffers



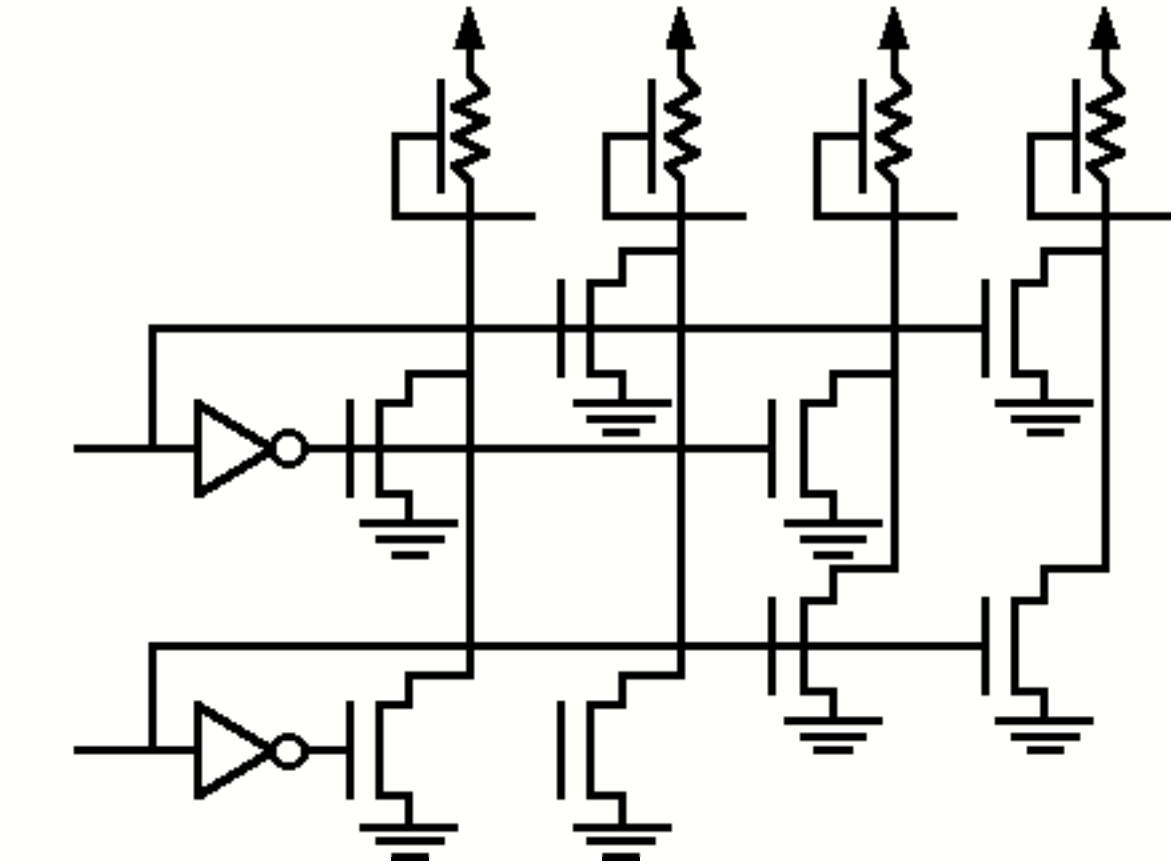
Inverting superbuffer

Non-inverting superbuffer

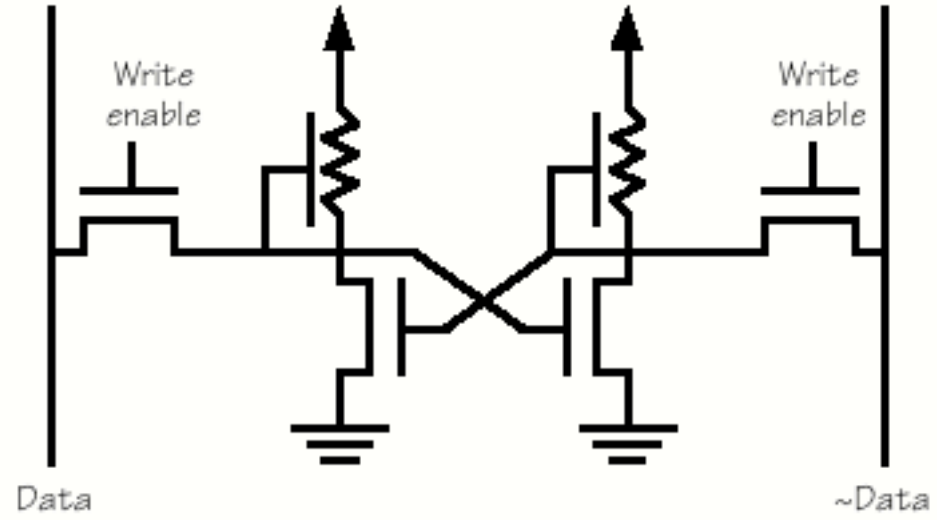
Decoder (NAND form)



Decoder (NOR form)

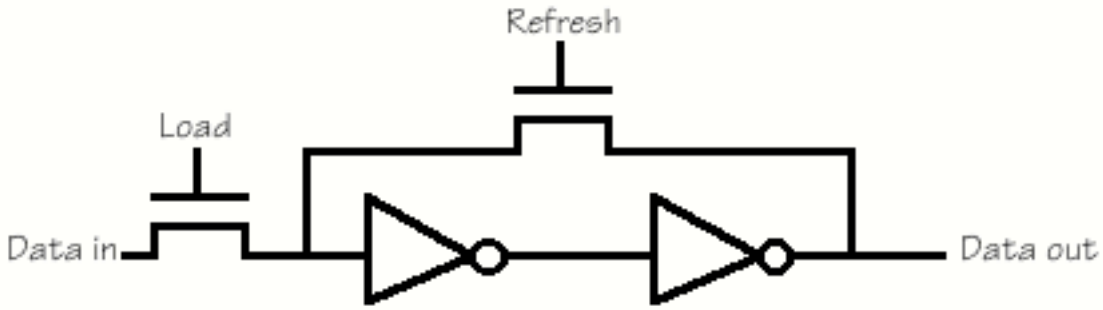


Six transistor static memory



- Data lines are used for both read and write
- Drive complementary data during write to set latch
- Need sense amplifiers - long wires

Six transistor dynamic memory cell



- Data is stored on gate capacitors
- Charge is slowly lost (leakage current)
- Need to periodically refresh data (~ 1 msec)
- Load and refresh on alternate clock phases
- 6-transistor design good for registers, not RAM
- Use 1-transistor design for large dynamic RAM