YAMAHA

YMW820 PRELIMINARY

NSX-1

■ Overview

YMW820 or NSX-1 is a sound generator device for consumer applications with wavetable synthesis core supporting up to 64 simultaneous voices. It already is a high-end ROM-based General MIDI- or GM-compliant sound module, and when waveforms are put on its large on-chip RAM it makes a wavetable synthesizer with the superb quality and expressiveness that can come close to real musical instruments.

It also integrates powerful RISC processor to control these sound generator cores, and it frees up the host controller from these chores.
The host controller may also load programs and wave samples on the on-chip RAM to extend NSX-1 with such features as VOCALOID--Yamaha's renowned singing synthesizer technology. And, the flexibility provided from having large set of power off- and power save-modes enables the device to be used in most products in today's portable device applications.

The information provided is preliminary, and subject to change without notice.
Please check for the latest information when using this product in your design.

YAMAHA CORPORATION

YMW820 CATALOG
CATALOG No. LSI-4MW820A00
2012.01

■ Features

- YMW820 is the sound generator device for consumer applications

[Sound Generator]

- Wavetable synthesis core supporting up to 64 simultaneous voices
  - · Sampling frequency : 44.1 kHz
  - · Large on-chip memories for waveforms
    - ➢ 2 Mbyte RAM (for typical use)
      The total 3 Mbyte of on-chip RAM can be partitioned into waveform storage (up to 2 Mbyte) and secondary work area for integrated CPU.
    - ➢ GM (General MIDI) sound presets ROM
  - · Integrated DSP for audio effect processing
  - · 2 digital audio inputs
    - ➢ Supports I^2S / Left-justified / Right-justified / PCM format
    - ➢ Sampling frequency : 8 kHz to 48 kHz
    - ➢ Supports both Master mode and Slave mode
  - · 2 digital audio outputs
    - ➢ Supports I^2S / Left-justified / Right-justified / PCM format
    - ➢ Sampling frequency : 8 kHz to 48 kHz
    - ➢ Supports both Master mode and Slave mode

[Integrated CPU]

- Powerful dual-issue 32-bit RISC processor
- Two selectable clock rates (135.4752 MHz or 67.7376 MHz)
- Caches (8 Kbyte for Instruction, 8 Kbyte for Data)
- Large integrated work memories
  - · Primary work area
    No wait accesses from the processor
  - · Secondary work area (1 Mbyte for typical use)
    The total 3 Mbyte of on-chip RAM can be partitioned into secondary work area (up to 3 Mbyte) and waveform storage.
- Integrated peripherals: DMAC, timer/counters, watchdog timer, and IRQ controller
- 3 programmable GPIO pins

- Sound Inputs and Outputs
  - · Integrated CPU accepts and processes sounds from the host controller, Sound Generator, and the one on the digital audio interface
  - · Integrated CPU outputs and Sound Generator outputs can be mixed
- Host Controller Interface
  - · Parallel 8- or 16-bit bus
  - · SPI. Supports 4 communication formats

    Mode 0: Positive pulse clocks; data sampled on rises, toggled on falls

    Mode 1: Positive pulse clocks; data toggled on rises, sampled on falls

    Mode 2: Negative pulse clocks; data sampled on falls, toggled on rises

    Mode 3: Negative pulse clocks; data toggled on falls, sampled on rises

[Package]

- Lead-free 80-pin SQFP package (YMW820-SZ)
- 12 mm×12 mm
- Pin pitch 0.5 mm

[Power Supply]

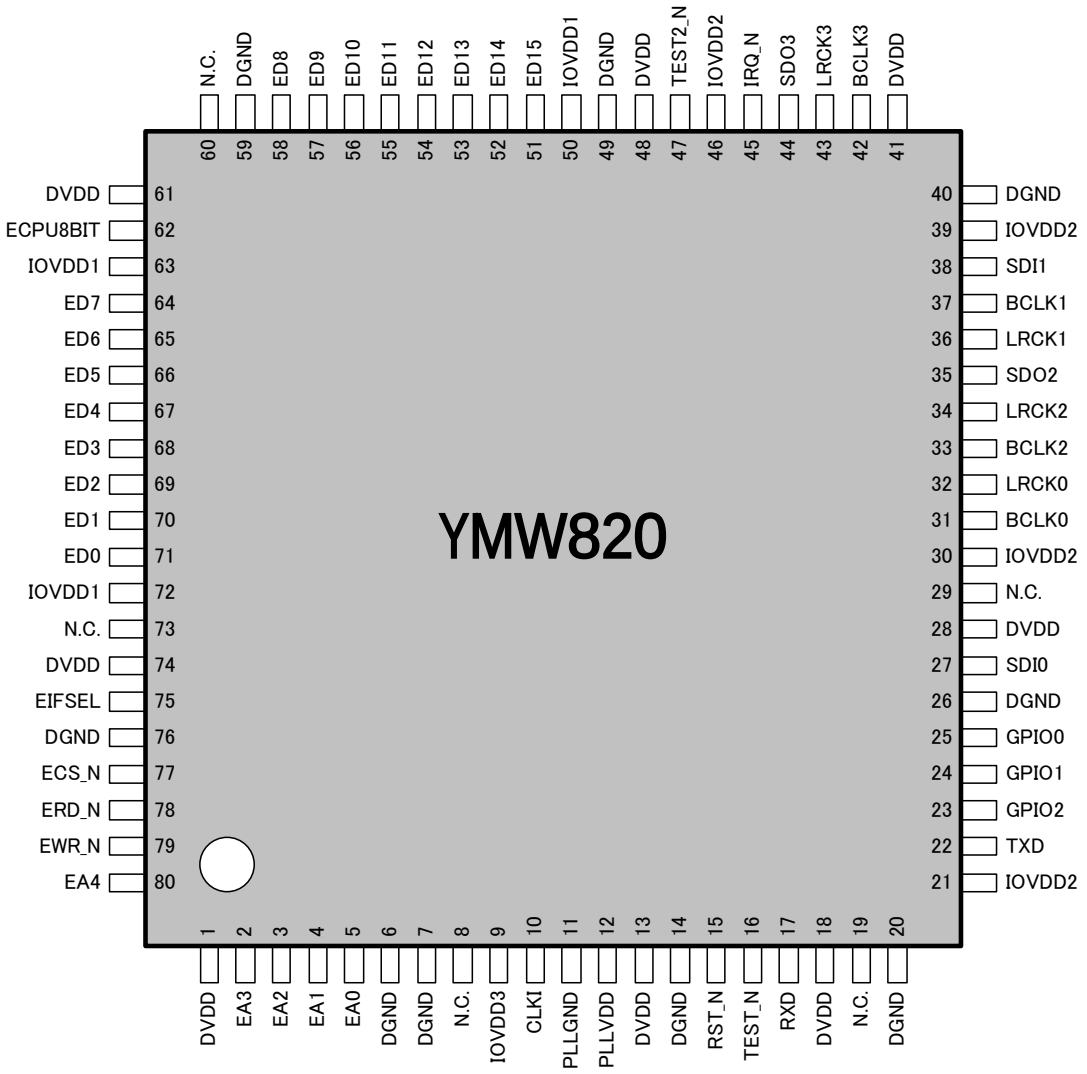
- Core supply (DVDD) :1.02 V to 1.20 V (1.10 V typical)
- I/O supply (IOVDD*) :1.65 V to 3.60 V

[Others]

- Power off- and Power save-modes
  Power consumption can be minimized with the large set of power off- and power save-modes

■ Pin Assignments

< Top View >



＜80pin SQFP Top View＞

■ Pin Descriptions

No.	Pin name	I/O	Power supply	Description
1	DVDD	P	−	Digital core supply (1.1 V)
2	EA3 / SPI_MODE	I	IOVDD1	(EIFSEL="L") Host controller parallel interface Address 3 (EIFSEL="H") SPI mode
3	EA2 / ESI	I	IOVDD1	(EIFSEL="L") Host controller parallel interface Address 2 (EIFSEL="H") SPI data input
4	EA1 / ESCK	I	IOVDD1	(EIFSEL="L")Host controller parallel interface Address 1 (EIFSEL="H") SPI clock input
5	EA0 / ESS_N	I	IOVDD1	(EIFSEL="L") Host controller parallel interface Address 0 (EIFSEL="H") SPI chip select
6	DGND	G	−	Digital core ground
7	DGND	G	−	Digital core ground
8	N.C.	N.C.	−	
9	IOVDD3	P	−	IO supply (1.65 V to 3.60 V)
10	CLKI	Ish/Itcxo	IOVDD3	Clock input (10 MHz to 27 MHz)
11	PLLGND	G	−	PLL ground
12	PLLVDD	P	−	PLL supply (1.1V)
13	DVDD	P	−	Digital core supply (1.1 V)
14	DGND	G	−	Digital core and IO ground
15	RST_N	Ish	IOVDD2	Hardware reset input
16	TEST_N	Ish	IOVDD2	Test pin
17	RXD	Ish	IOVDD2	Receive data input
18	DVDD	P	−	Digital core supply (1.1 V)
19	N.C.	N.C.	−	
20	DGND	G	−	Digital core and IO ground

No.	Pin name	I/O	Power supply	Function	
21	IOVDD2	P	—	IO supply (1.65 V to 3.60 V)	
22	TXD	O	IOVDD2	Transmit data output	
23	GPIO2	I/O	IOVDD2	GPIO	
24	GPIO1	I/O	IOVDD2	GPIO	
25	GPIO0	I/O	IOVDD2	GPIO	
26	DGND	G	—	Digital core and IO ground	
27	SDI0	I	IOVDD2	Digital audio interface #0	input data
28	DVDD	P	—	Digital core supply (1.1 V)	
29	N.C.	N.C.	—		
30	IOVDD2	P	—	IO supply (1.65 V to 3.60 V)	
31	BCLK0	I/O	IOVDD2	Digital audio interface#0	Bit clock
32	LRCK0	I/O	IOVDD2	Digital audio interface#0	LR clock
33	BCLK2	I/O	IOVDD2	Digital audio interface#2	Bit clock
34	LRCK2	I/O	IOVDD2	Digital audio interface#2	LR clock
35	SDO2	O	IOVDD2	Digital audio interface#2	Output data
36	LRCK1	I/O	IOVDD2	Digital audio interface#1	LR clock
37	BCLK1	I/O	IOVDD2	Digital audio interface#1	Bit clock
38	SDI1	I	IOVDD2	Digital audio interface#1	Input data
39	IOVDD2	P	—	IO supply (1.65 V to 3.60 V)	
40	DGND	G	—	Digital core and IO ground	

No.	Pin name	I/O	Power supply	Function	
41	DVDD	P	—	Digital core supply (1.1 V)	
42	BCLK3	I/O	IOVDD2	Digital audio interface#3	Bit clock
43	LRCK3	I/O	IOVDD2	Digital audio interface#3	LR clock
44	SDO3	O	IOVDD2	Digital audio interface#3	Output data
45	IRQ_N	O	IOVDD2	Interrupt request	
46	IOVDD2	P	—	IO supply (1.65 V to 3.60 V)	
47	TEST2_N	Ish	IOVDD2	Test pin. Always tied to DGND.	
48	DVDD	P	—	Digital core supply (1.1 V)	
49	DGND	G	—	Digital core and IO ground	
50	IOVDD1	P	—	IO supply (1.65 V to 3.60 V)	
51	ED15	I/O	IOVDD1	Host controller parallel interface	Data 15
52	ED14	I/O	IOVDD1	Host controller parallel interface	Data 14
53	ED13	I/O	IOVDD1	Host controller parallel interface	Data 13
54	ED12	I/O	IOVDD1	Host controller parallel interface	Data 12
55	ED11	I/O	IOVDD1	Host controller parallel interface	Data 11
56	ED10	I/O	IOVDD1	Host controller parallel interface	Data 10
57	ED9	I/O	IOVDD1	Host controller parallel interface	Data 9
58	ED8	I/O	IOVDD1	Host controller parallel interface	Data 8
59	DGND	G	—	Digital core and IO ground	
60	N.C.	N.C.	—		

No.	Pin name	I/O	Power supply	Function	
61	DVDD	P	－	Digital core supply (1.1 V)	
62	ECPU8BIT	I	IOVDD1	Host controller parallel interface	Bus width select
63	IOVDD1	P	－	IO supply (1.65 V to 3.60 V)	
64	ED7	I/O	IOVDD1	Host controller parallel interface	Data 7
65	ED6	I/O	IOVDD1	Host controller parallel interface	Data 6
66	ED5	I/O	IOVDD1	Host controller parallel interface	Data 5
67	ED4	I/O	IOVDD1	Host controller parallel interface	Data 4
68	ED3	I/O	IOVDD1	Host controller parallel interface	Data 3
69	ED2	I/O	IOVDD1	Host controller parallel interface	Data 2
70	ED1	I/O	IOVDD1	Host controller parallel interface	Data 1
71	ED0	I/O	IOVDD1	Host controller parallel interface	Data 0
72	IOVDD1	P	－	IO supply (1.65 V to 3.60 V)	
73	N.C.	N.C.	－		
74	DVDD	P	－	Digital core supply (1.1 V)	
75	EIFSEL	I	IOVDD1	Host controller: parallel interface / SPI select	
76	DGND	G	－	Digital core and IO ground	
77	ECS_N	I	IOVDD1	Host controller parallel interface	Chip select
78	ERD_N	I	IOVDD1	Host controller parallel interface	Read
79	EWR_N / ESO	I/O	IOVDD1	(EIFSEL=“L”) Host controller parallel interface	Write
				(EIFSEL=“H”) SPI	Data Output
80	EA4 / HOLD_N	I	IOVDD1	(EIFSEL=“L”) Host controller parallel interface	Address 4
				(EIFSEL=“H”)SPI	Hold

Symbols	
I	Digital input
O	Digital output
I/O	Digital input and output
Ish	Digital input (Schmitt trigger input)
Itcxo	Digital input(TCXO)
P	Power supplies
G	GND
N.C.	No Connect (pin is not connected anywhere in the device)

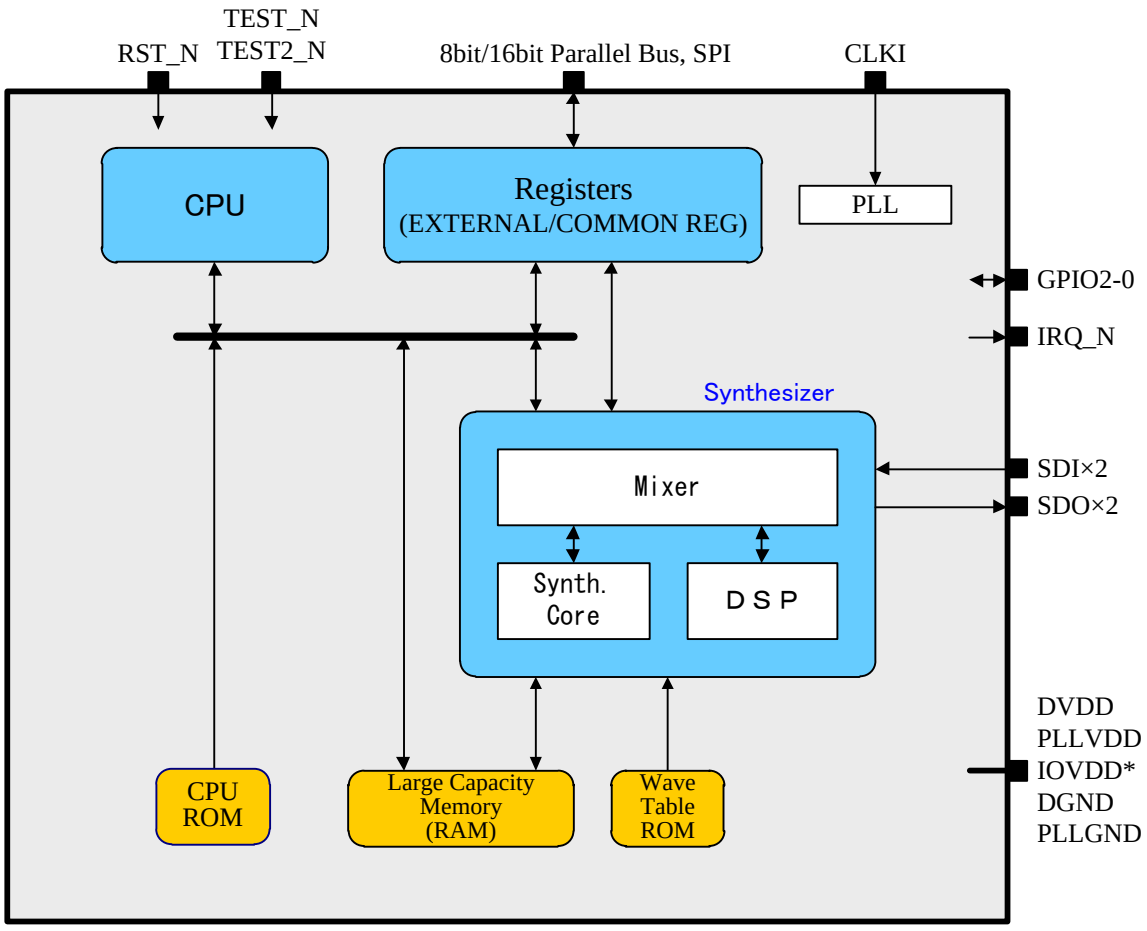
N.C.: No Connect

No problem occurs even if connected to a supply voltage line, a ground line, or a signal line on a board. In addition, connection to an independent land pattern that is electrically unconnected also does not cause any problem.

All the power lines are electrically separated.

And, all the GND pins are connected via the substrate in the device.

■ Block Diagram



<Registers>

Registers block contains registers and interface circuitry for the host controller communication.
YMW820 supports 8- or 16-bit parallel bus and SPI bus as the host controller interface.
This block also provides access ports for internal YMW820 registers such as COMMON REG, COMMAND FIFO, and the host can read and write those registers through these ports.

<CPU>

CPU is the integrated data processing application platform based on powerful dual-issue 32-bit RISC processor core and bus-based architecture.
Peripheral functions such as Timer, DMA controller, Interrupt controller are also integrated on chip.

<Synthesizer>

Synthesizer is the wavetable synthesis core supporting up to 64 simultaneous voices. It also contains DSP for sound effect processing which is controlled from the integrated CPU.

<Digital Audio Interface [Input]>

Digital Audio Interface block provides two input ports in digital audio interface data format, and these ports can also be used in PCM interface data format.
For digital audio interface data format, it supports input of 16/20/24-bit samples in 2's complement representation at one of 9 sampling rates between 8 kHz and 48 kHz.
For PCM interface data format, it supports 8/13/14/16-bit samples at 8 kHz or 16 kHz sampling rate.
YMW820 can operate as either master or slave input device for both data formats.
As a slave device, it automatically determines and uses one of the 9 supported sampling rates.
Once inside the device, further processing can be applied to these audio samples.

<Digital Audio Interface [Output]>

Digital audio interface block provides two output ports in digital audio interface data format, and these ports can also be used in PCM interface data format.
For digital audio input interface data format, it supports output of 16/20/24-bit samples in 2's complement representation at one of 9 sampling rates between 8 kHz and 48 kHz.
For PCM interface data format, it supports output of 8/13/14/16-bit samples at 8 kHz or 16 kHz sampling rate.
YMW820 can operate as either master or slave output device for both data formats.
As a slave device, it automatically determines and uses one of the 9 supported sampling rates.

<PLL, Clock Generator>

CLKI pin of this block accepts standard CMOS level inputs, and in *TCXO mode* also accepts a low amplitude inputs.
PLL block generates system clocks used in YMW820 from the clock signal on CLKI pin.

■ Electrical Characteristics

● Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
DVDD Supply Voltage	DVDD	−0.3	1.40	V
PLLVDD Supply Voltage	PLLVDD	−0.3	1.40	V
IOVDD1 Supply Voltage	IOVDD1	−0.3	4.20	V
IOVDD2 Supply Voltage	IOVDD2	−0.3	4.20	V
IOVDD3 Supply Voltage	IOVDD3	−0.3	4.20	V
Digital Input Voltage(1) (*1) (*4)	VIND1	−0.3	IOVDD1+0.3	V
Digital Input Voltage(2) (*2) (*4)	VIND2	−0.3	IOVDD2+0.3	V
Digital Input Voltage(3) (*3) (*4)	VIND3	−0.3	IOVDD3+0.3	V
Power Dissipation (*5)	Pd		203	mW
Storage Temperature	TSTG	−50	125	℃

[Conditions] DGND = PLLGND = 0 V

(*1) For input pins and input/output pins that run from IOVDD1 supply.

(*2) For input pins and input/output pins that run from IOVDD2 supply.

(*3) For input pins and input/output pins that run from IOVDD3 suppy.

(*4) The value is applicable even if the supply voltages are outside the recommended operationg range.
e.g., When power supply pins are at 0 V, voltages over 0.3 V do not meet the rating.

(*5) For Top = 25°C, PCB (76.2 mm × 114.3 mm × 1.6 tmm), glass-reinforced epoxy PCB board.
When operating above Top = 25°C, derate the value by 2.03 mW per 1°C.
The value is of approximate nature, as it was obtained by a simulation program assuming a certain condition.

● Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
DVDD, PLLVDD Operating Voltage (*1)	DVDD	1.02	1.10	1.20	V
IOVDD1 Operating Voltage	IOVDD1	1.65	1.80	3.60	V
IOVDD2 Operating Voltage	IOVDD2	1.65	1.80	3.60	V
IOVDD3 Operating Voltage	IOVDD3	1.65	1.80	3.60	V
Operating Ambient Temperature	TOP	-20	25	85	℃

[Conditions] DGND = PLLGND = 0 V

(*1) PLLVDD must be connected to DVDD through a discrete resistor external to YMW820.

● Power Consumptions

Parameter	Condition	Typ. (*1)	Max. (*2)	Unit
DVDD + PLLVDD	Normal Operation (*4) (CPU_FREQ="0") (CPU_FREQ="1")	 35 25		mA
IOVDD1	Normal Operation (*4)	0.5		mA
IOVDD2	Normal Operation (*5)	0.8		mA
IOVDD3	Normal Operation (CMOS mode)	0.1		mA
	Normal Operation (TCXO mode)	0.1		mA
Power-off mode (*3)	Total power supply current	20	60	μA
Power-save mode (*3)	Total power supply current	450	1800	μA

(*1) With the *typical* values of voltages specified in the recommended operating conditions, and at TOP = 25°C.
(*2) With the *maximum* values of voltages specified in the recommended operating conditions, and at TOP = 25°C.
(*3) ECS_N input pin (V_{IH} = IOVDD1 fixed); other input pins (V_{IL} = DGND, V_{IH} = IOVDD1, IOVDD2, IOVDD3)
(*4) For playback of sample sound contents using the on-chip GM sound presets as well as high-quality waveforms downloaded from the host on the on-chip wave memory.
(*5) DIR, DIT setting: fs = 48.0 kHz, BCLK = 64 fs, Master mode

● DC characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage "H" Level 1	V_{IH}	(*1)	0.70 × IOVDD1			V
Input Voltage "L" Level 1	V_{IL}	(*1)			0.30 × IOVDD1	V
Input Voltage "H" Level 2	V_{IH}	(*2)	0.70 × IOVDD2			V
Input Voltage "L" Level 2	V_{IL}	(*2)			0.30 × IOVDD2	V
Input Voltage "H" Level 3	V_{IH}	(*3)	0.75 × IOVDD2			V
Input Voltage "L" Level 3	V_{IL}	(*3)			0.25 × IOVDD2	V
Input Voltage "H" Level 4	V_{IH}	(*4)	0.75 × IOVDD3			V
Input Voltage "L" Level 4	V_{IL}	(*4)			0.25 × IOVDD3	V
Output Voltage "H" Level 1	V_{OH}	(*1) (*5)	0.80 × IOVDD1			V
Output Voltage "L" Level 1	V_{OL}	(*1) (*5)			0.20 × IOVDD1	V
Output Voltage "H" Level 2	V_{OH}	(*2) (*5)	0.80 × IOVDD2			V
Output Voltage "L" Level 2	V_{OL}	(*2) (*5)			0.20 × IOVDD2	V
Schmitt Trigger Trip Point Range 1	V_{sh1}	TEST_N, TEST2_N, RST_N, RXD		0.05 × IOVDD2		V
Schmitt Trigger Trip Point Range 2	V_{sh2}	CLKI (*4)		0.05 × IOVDD3		V
Input Leakage Current	IL				±1.0	μA
Input Capacitance	CI				10	pF

[Conditions] With the Recommended Operating Conditions, and capacitive load of 50 pF.
(*1) For pins running from IOVDD1 supply.
(*2) For pins: SDI*, LRCK*, BCLK*, GPIO*.
(*3) For pins: RST_N, TEST_N, TEST2_N, RXD.
(*4) For pins: CLKI (in CMOS mode).
(*5) For BCLK*, GPIO*: I_{OH} = −2 mA, I_{OL} = +2 mA, other output pins: I_{OH} = −1 mA, I_{OL} = +1 mA.
For other output pins: I_{OH} = −0.2 mA, I_{OL} = +0.2 mA (when IOVDD1, IOVDD2 is less than 2.20 V)

● AC Characteristics

• Power Up and Reset Sequences, and Input Signal Rise/Fall Time

Parameter	Symbol	Min.	Typ.	Max.	Unit
RST_N "L" pulse width (*1)	T_{RSTW}	1			µs
RST_N setup (for undefined → L) time (*2)	T_{RSTS}	0			µs
Power supply ramp time (*3)	T_{VRISE}			10	ms
Power-up timing skew between power supplies (*4)	T_{VSKW}	0		5	ms
Rise and fall time of inputs except CLKI, RST_N	T_r, T_f			20	ns

[Conditions] With the Recommended Operating Conditions.

(*1) This value is specified for the timing of RST_N signal and the last supply to become valid among DVDD, IOVDD1 through 3. The timing of PLLVDD is outside the consideration.

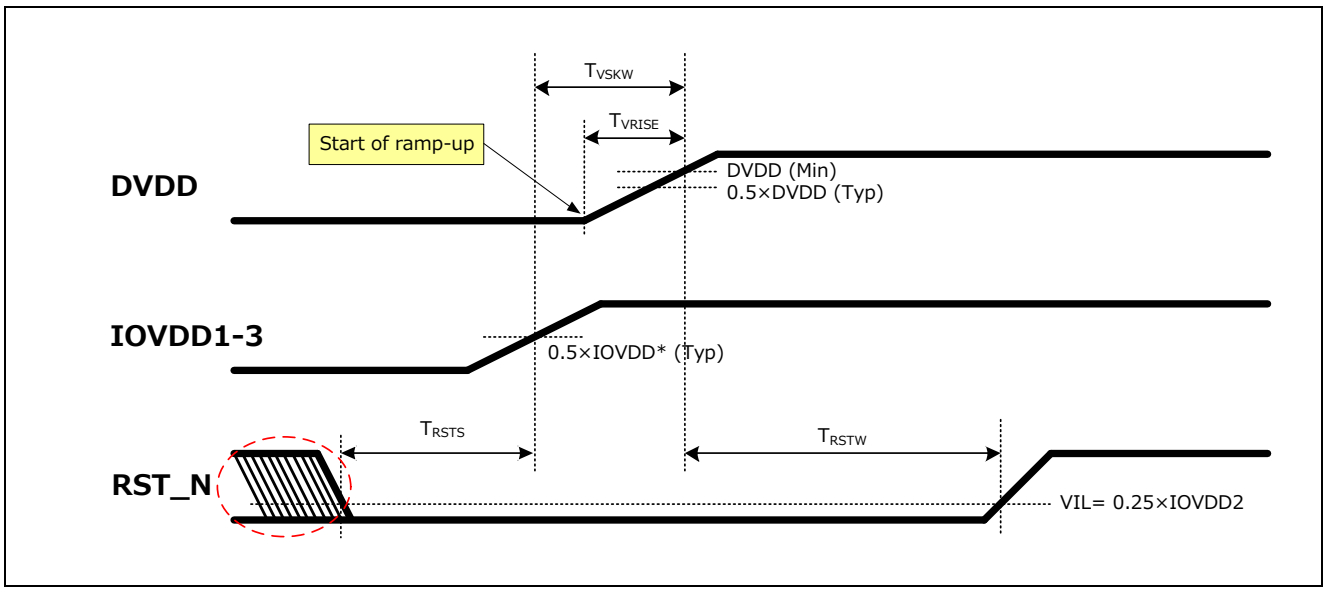
(*2) Specified for the timings of IOVDD2 ramp-up and RST_N signal.

(*3) Specified the ramp time for power supplies.
(It is the time from the start of supply until the minimum voltage in the Recommended Operating Condition is reached.) Diagram below shows only DVDD timing, although the specification applies to IOVDD1 through 3.

(*4) This value is specified for the ramp-up timings of the first and the last suppies to become valid among DVDD and IOVDD1 through 3.

Timing Diagram For When IOVDD* Comes up Before DVDD

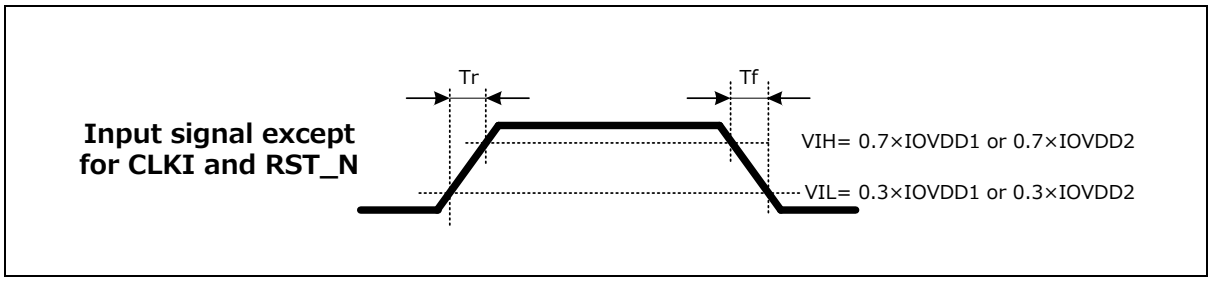
Power sequencing among DVDD and IOVDDs supplies is not specified for this device. In timing diagram below IOVDDs come up before DVDD (and IOVDD1 through 3 come up at the same time).



- DVDD (Min.) is the minimum value specified in the Recommended Operating Conditions.
- DVDD (Typ.) and IOVDD* (Typ.) are the typical values specified in the Recommended Operating Conditions.
- RST_N signal must stay within the range specified in the Absolute Maximum Ratings even while the signal is not driven and the device is not powered.

(*) Although particular power sequencing is not required, we recommend the following.

1. Turn on IOVDDs. (No particular order requested for IOVDD1 through IOVDD3)
2. Turn on DVDD.
3. Release the reset signal (RST_N = “H”).



Notes on RST_N signal during power supply ramp-up

RST_N pin must be driven low when IOVDD2 supply ramps up or earlier.
IO directions of the bidirectional pins that run from IOVDD2 supply and output levels of the output pins that run from IOVDD2 supply get ready when RST_N is low and IOVDD2 reach its valid range.

IO directions of ED15 through ED0 pins get set by the logic levels of ECS_N and ERD_N which run from IOVDD1 supply. (The levels of ECS_N and ERD_N do not affect the direction of ED15 through ED8 which always become input pins when ECPU8BIT is high, that is, when the bus width is 8-bit)
IO directions of ED15-ED0 get set with valid IOVDD1 even before DVDD ramps up. (ECS_N is recommended to be driven low when IOVDD1 ramps up).

• Clock Input (CLKI)

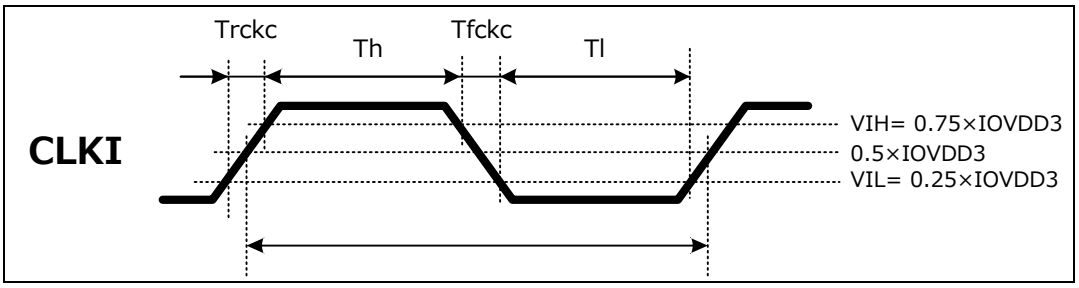
i) CMOS Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLKI frequency	1 / Tfreq	10		27	MHz
CLKI rise / fall time	Trckc, Tfckc			30	ns
CLKI high time	Th	15			ns
CLKI low time	Tl	15			ns
Acceptable frequency deviation range	-			±100	ppm

[Conditions] With the Recommended Operating Conditions.

Clock signals to CLKI can be stopped (= 0 Hz) and fixed to a level in Power-off and Power-save mode, and during the device reset.

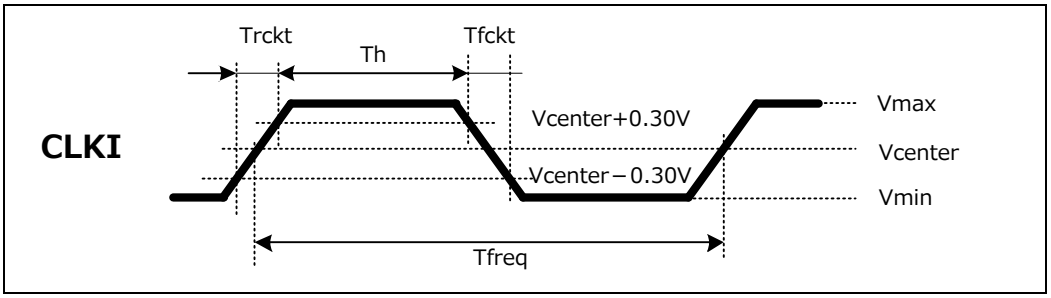
・When DVDD and IOVDDs come from different supplies, ramp up DVDD first.



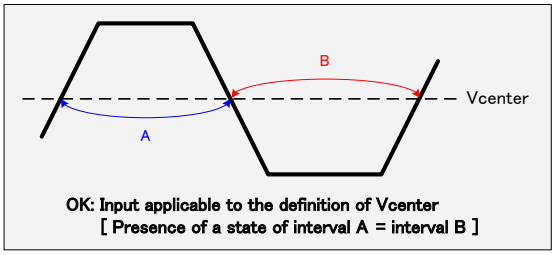
ii) TCXO Mode

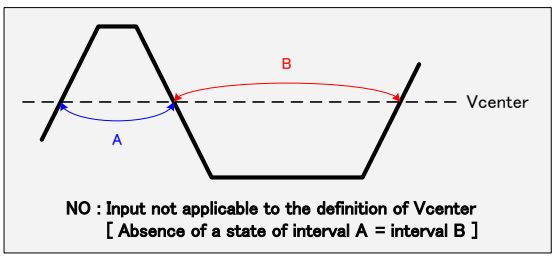
Parameter	Symbol	Min.	Typ.	Max.	Unit
CLKI frequency	1 / Tfreq	10		27	MHz
CLKI rise/ fall time	Trckt, Tfckt			50	ns
CLKI amplitude H (*1)	Vmax－Vcenter	0.20		0.35× IOVDD3	V
CLKI amplitude L (*1)	Vcenter－Vmin	0.20		0.35× IOVDD3	V
Wait time to stable (*1)	Twait	2			ms
Feedback resistance	Rck	13.5	27	54	kΩ
Acceptable frequency deviation range	-			±100	ppm

[Conditions] With the Recommended Operating Conditions.
(*1) TCXO module's output is assumed to be AC-coupled to CLKI using a 1000 pF capacitor.
The AC-coupling capacitor must be 1000 pF for this application.



- *Vcenter* is defined as the voltage level of TCXO signals at which the duty cycles of CLKI become 50% (High time = Low time).
  When Vcenter cannot be defined as above for a waveform, for example, when there are too much high/low time disparities, the use of such waveforms as CLKI is prohibited.
- *Trckt* and *Tfckt* are specified as a transition time between the two reference signal levels, Vcenter + 0.30 [V] and Vcenter – 0.30 [V].
- *Tfreq* is specified as a cycle period using the reference level at Vcenter (Duty = 50%).





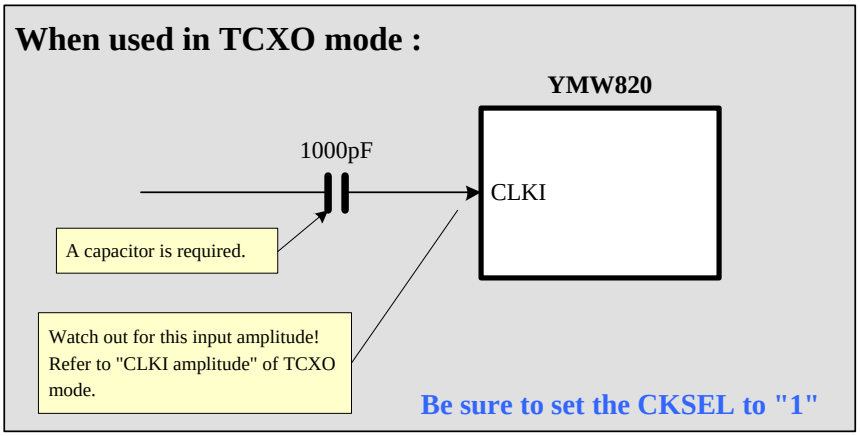
iii) Design note on CLKI clock input networks

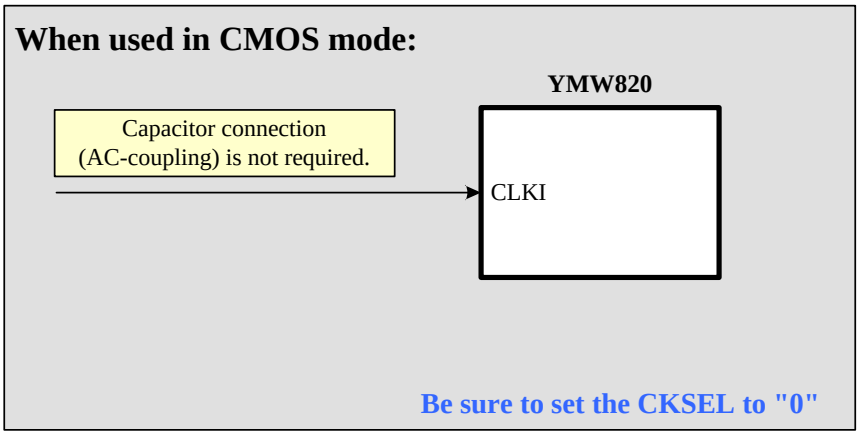
CKSEL configures if YMW820 operates in TCXO mode or CMOS mode.

Notice that external networks for CLKI pin and the expected clock signal characteristics are different for each mode. Section *Clock Input (CLKI)* for the signal characteristics.

Refer to “Input Clock (CLKI)” for the details of the characteristics of CLKI pin's input signals.

CKSEL configuration, and the external network and the expected clock signal characteristics on CLKI pin must be consistent with each other.





• Host Controller Interface Timing (8-bit, 16-bit parallel bus)

Followings are the conditions assumed for the specified values.

Input logic voltage levels : V_{IH} = 0.80 × IOVDD1, V_{IL}=0.20 × IOVDD1

Input, output timing reference levels : V_{IH} = 0.70 × IOVDD1, V_{IL}= 0.30 × IOVDD1

V_{OH} =0.70 × IOVDD1, V_{OL}=0.30 × IOVDD1

Write Cycle

Parameter	Symbol	Min.	Max.	Unit
Address setup time	T_{ADS}	30		ns
Address hold time	T_{ADH}	0		ns
Chip select setup time	T_{CSS}	30		ns
Chip select hold time	T_{CSH}	0		ns
Write pulse width	T_{WW}	30		ns
Data setup time	T_{WDS}	20		ns
Data hold time	T_{WDH}	0		ns

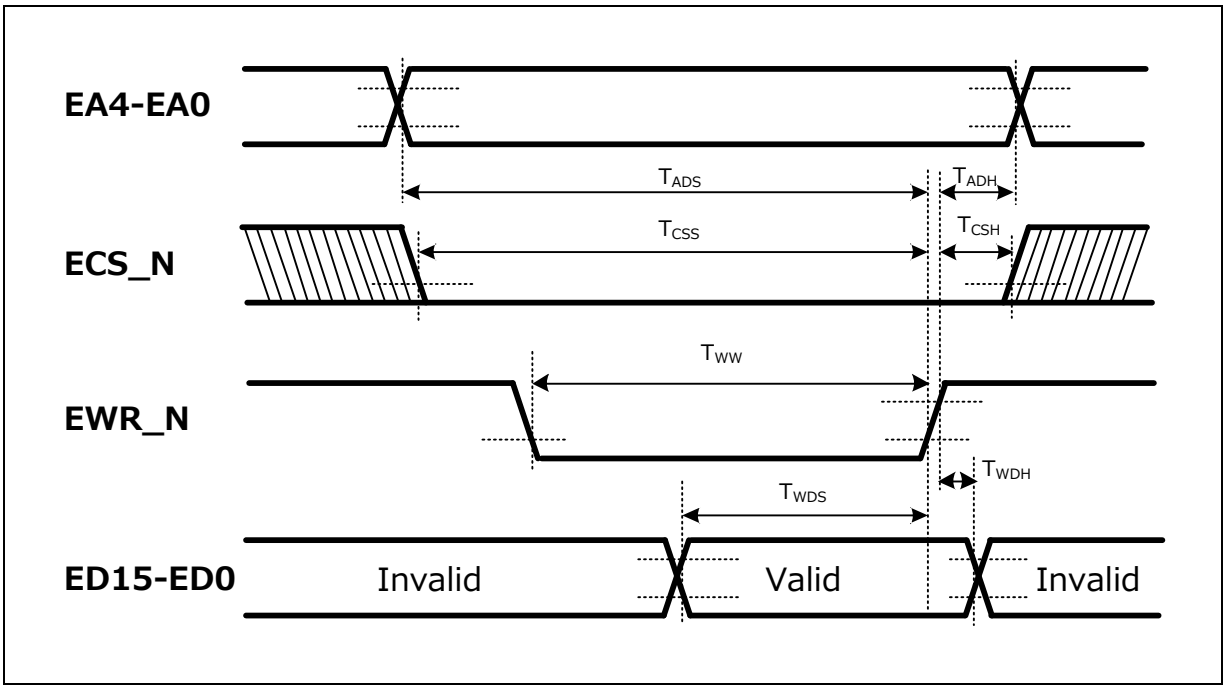
Read Cycle

Parameter	Symbol	Min.	Max.	Unit
Address hold time	T_{ADH}	0		ns
Chip select hold time	T_{CSH}	0		ns
Access time from ERD_N pin (ECPU_DRVS="0") (ECPU_DRVS="1")	T_{ACCRD}		 50 60	ns
Access time from ECS_N pin (ECPU_DRVS="0") (ECPU_DRVS="1")	T_{ACCCS}		 50 70	ns
Access time from EA4 - EA0 pin (ECPU_DRVS="0") (ECPU_DRVS="1")	T_{ACCAD}		 50 60	ns
Data hold time from ERD_N pin	T_{DHRD}	0		ns
High-impedance transition time from ERD_N pin	T_{DZRD}		15	ns

[Conditions] With the Recommended Operating Conditions, and capacitive load of 50 pF

I_{OH}, I_{OL} = 0 mA

i) Timing Diagram for Write Operations



Notes:

T_{ADH} : EA4-EA0 hold time relative to the 0.70×IOVDD1 reference timing point of rising EWR_N assuming both T_{CSH} and T_{WDH} meet the minimum value of 0 ns.

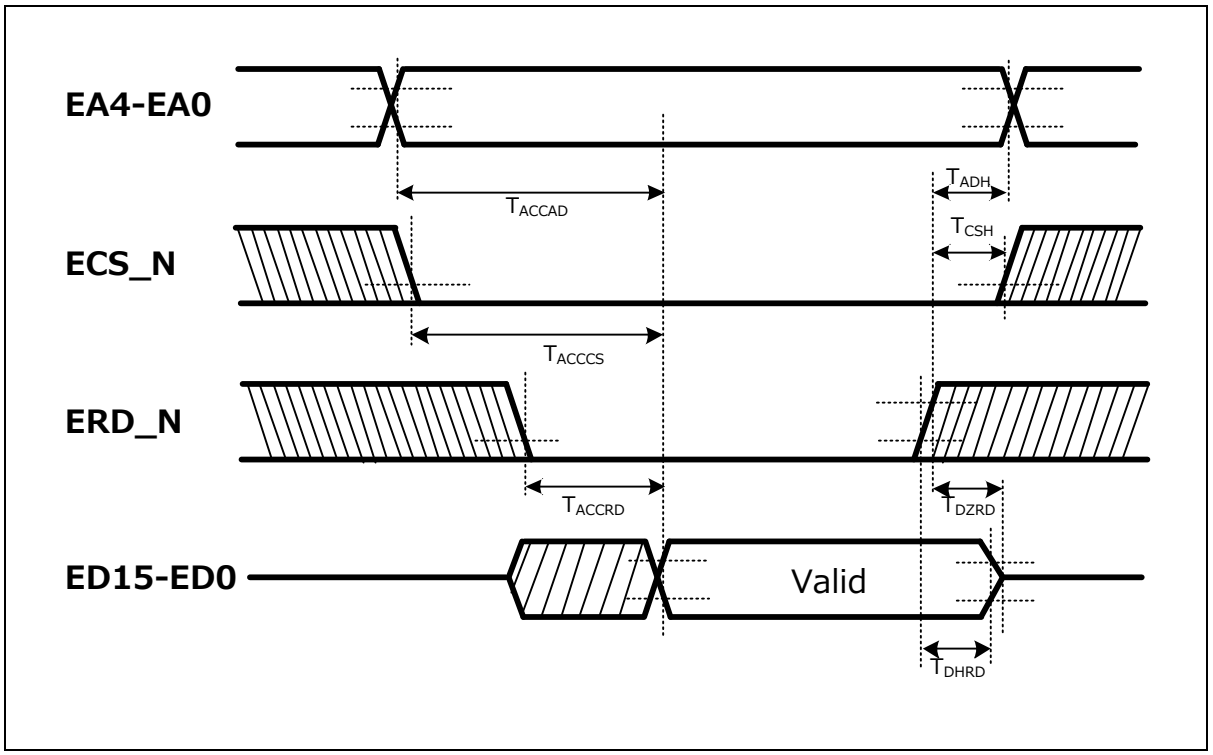
T_{CSH} : ECS_N hold time relative to the 0.70×IOVDD1 reference timing point of rising EWR_N assuming both T_{ADH} and T_{WDH} meet the minimum value of 0 ns.

T_{WDH} : ED15-ED0 hold time relative to the 0.70×IOVDD1 reference timing point of rising EWR_N assuming both T_{ADH} and T_{WDH} meet the minimum value of 0 ns.

T_{ADS} : EA4-EA0 setup time relative to the 0.30×IOVDD1 reference timing point of rising EWR_N assuming all of T_{CSS}, T_{WW}, and T_{WDS} meet the minimum value.

T_{CSS} : ECS_N setup time relative to the 0.30×IOVDD1 reference timing point of rising EWR_N assuming all of T_{ADS}, T_{WW}, and T_{WDS} meet the minimum value.

ii) Timing Diagram for Read Operations



Notes:

T_{ACCAD} : Access time from EA4-EA0 reaching 0.70×IOVDD1 or 0.30×IOVDD1, to ED15-ED0 reaching 0.70×IOVDD1 or 0.30×IOVDD1, assuming ERD_N and ECS_N become valid *in time* (*1).

T_{ACCCS} : Access time from ECS_N reaching 0.30×IOVDD1, to ED15-ED0 reaching 0.70×IOVDD1 or 0.30×IOVDD1, assuming EA4-EA0and ERD_N become valid *in time* (*1).

T_{ACCRD} : Access time from ERD_N reaching 0.30×IOVDD1, to ED15-ED0 reaching 0.70×IOVDD1 or 0.30×IOVDD1, assuming EA4-EA0 and ECS_N become valid *in time* (*1).

T_{DHRD} : ED15-ED0 hold time relative to the 0.30×IOVDD1 reference timing point of rising ERD_N assuming both T_{ADH} and T_{CSH} are 0 ns or more.

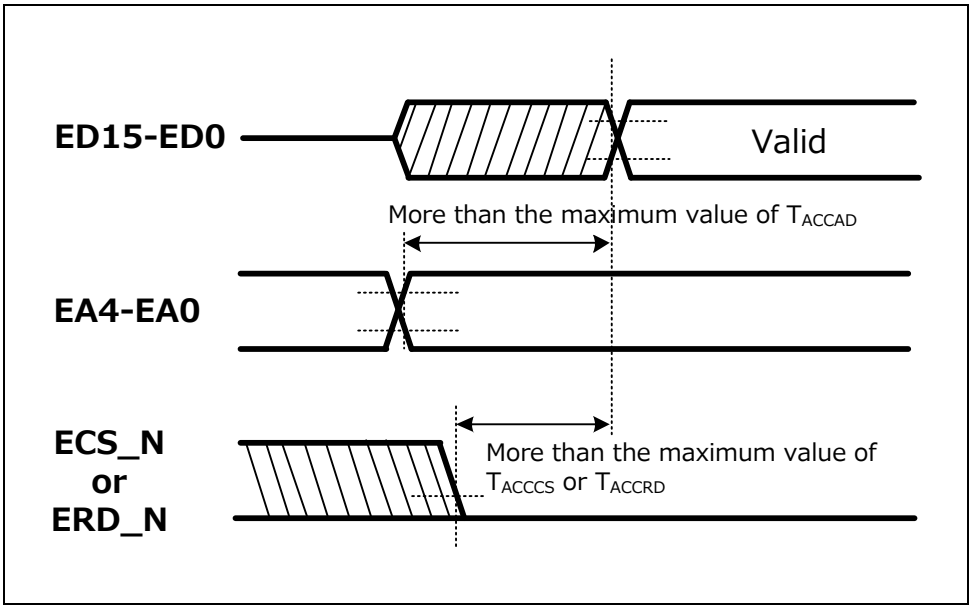
T_{DZRD} : ED15-ED0 transition time, into the high impedance states, relative to the 0.70×IOVDD1 reference timing point of rising ERD_N assuming both T_{ADH} and T_{CSH} are 0 ns or more.

(*1) *in time* Means:

For ECS_N : ECS_N has reached 0.30 × IOVDD1 T_{ACCCS} or more before ED15-ED0 all reaching 0.70 × IOVDD1 or 0.30 × IOVDD1.

For ERD_N : ERD_N has reached 0.30 × IOVDD1 T_{ACCRD} or more before ED15-ED0 all reaching 0.70 × IOVDD1 or 0.30 × IOVDD1.

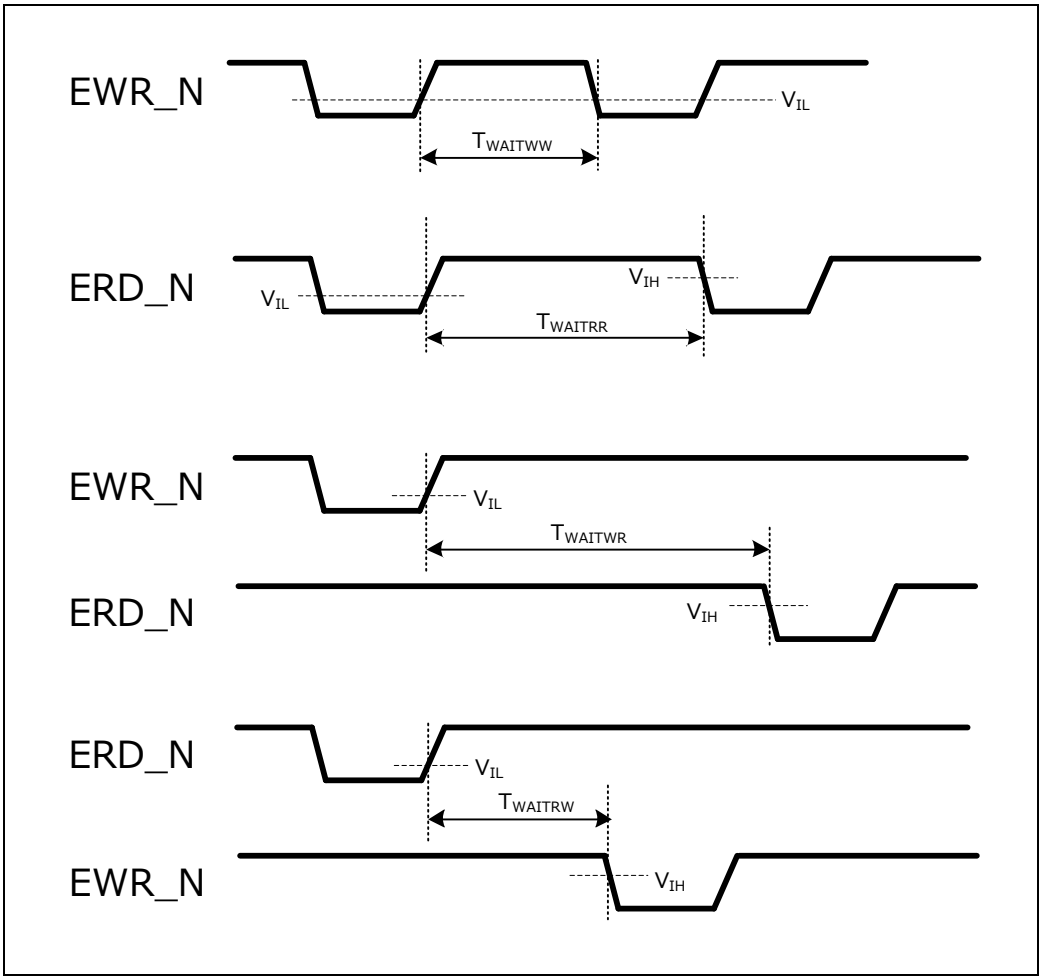
For EA4-EA0 : EA4-EA0 have reached 0.70 × IOVDD1 or 0.30 × IOVDD1 T_{ACCAD} or more before ED15-ED0 all reaching 0.70 × IOVDD1 or 0.30 × IOVDD1.



iii) Access Wait State

Parameter	Symbol	Min.	Max.	Unit
Write – Write access sequence wait time				
(First write after software RESET) (*1)	T_{WAITWW}	200		ns
(Other than above)	T_{WAITWW}	30		ns
Read – Read access sequence wait time	T_{WAITRR}	120		ns
Write – Read access sequence wait time				
(First read after software RESET) (*1)	T_{WAITWR}	150		ns
(Other than above)	T_{WAITWR}	120		ns
Read – Write access sequence wait time	T_{WAITRD}	30		ns

(*1) Wait time for the first read or write operation following a write to EXTERNAL REG 0x0E RESET.



• Host Controller Interface Timing (SPI)

Followings are the conditions assumed for the specified values.

Input logic voltage levels : V_{IH} = 0.80 × IOVDD1, V_{IL}=0.20 × IOVDD1

Input, output timing reference levels : V_{IH} = 0.70 × IOVDD1, V_{IL}= 0.30 × IOVDD1

V_{OH} =0.70 × IOVDD1, V_{OL}=0.30 × IOVDD1

Input timing

Parameter	Symbol	Min.	Max.	Unit
ESCK frequency (Write access) (*1)	F_C		40	MHz
ESCK frequency (Read access) (*1) (ECPU_DRVS="0") (ECPU_DRVS="1")	F_{CR}		 15 10	MHz
ESCK “H” pulse width	T_{CH}	10		ns
ESCK “L” pulse width	T_{CL}	10		ns
ESCK rise time (*1)	T_{CLCH}		5	ns
ESCK fall time (*1)	T_{CHCL}		5	ns
ESS_N setup time	T_{SSU}	15		ns
ESS_N hold time	T_{SHD}	15		ns
ESI setup time	T_{DSU}	5		ns
ESI hold time	T_{DHD}	10		ns
HOLD_N setup time	T_{HSU}	10		ns
HOLD_N hold time	T_{HHD}	10		ns
ESS_N “H” pulse width	T_{SW}	20		ns

(*1) Maximum ESCK rise time and fall time cannot be made to fit the cycle period for the maximum ESCK frequency.

Output timing

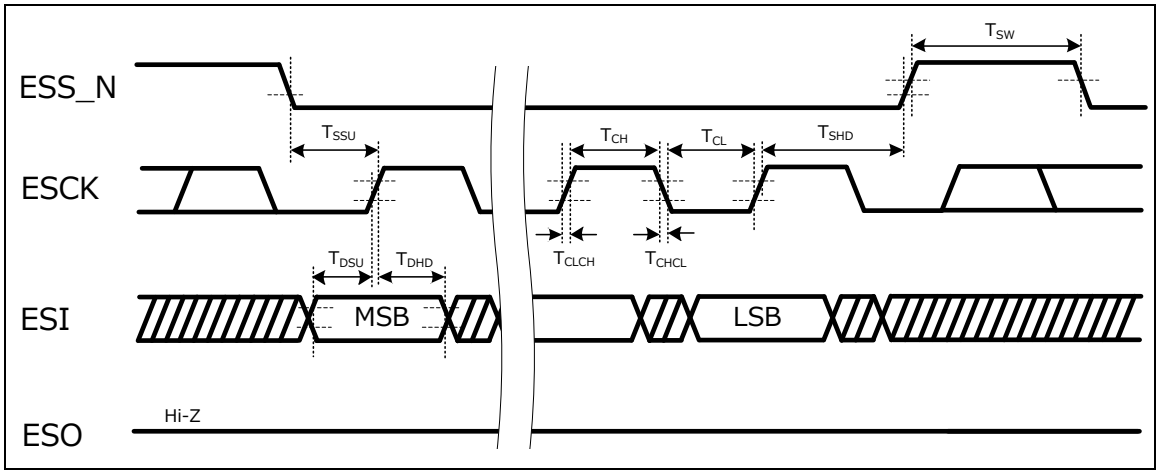
Parameter	Symbol	Min.	Max.	Unit
Access time (ECPU_DRVS="0") (ECPU_DRVS="1")	T_{QV}		 30 40	ns
Data hold time	T_{QX}	2		ns
High-impedance transition time	T_{QZ}		10	ns
Access time (HOLD_N=“L”) (ECPU_DRVS="0") (ECPU_DRVS="1")	T_{HV}		 30 40	ns
High-impedance transition time (HOLD_N=“L”)	T_{HZ}		15	ns

[Conditions] With the Recommended Operating Conditions, and capacitive load of 30 pF

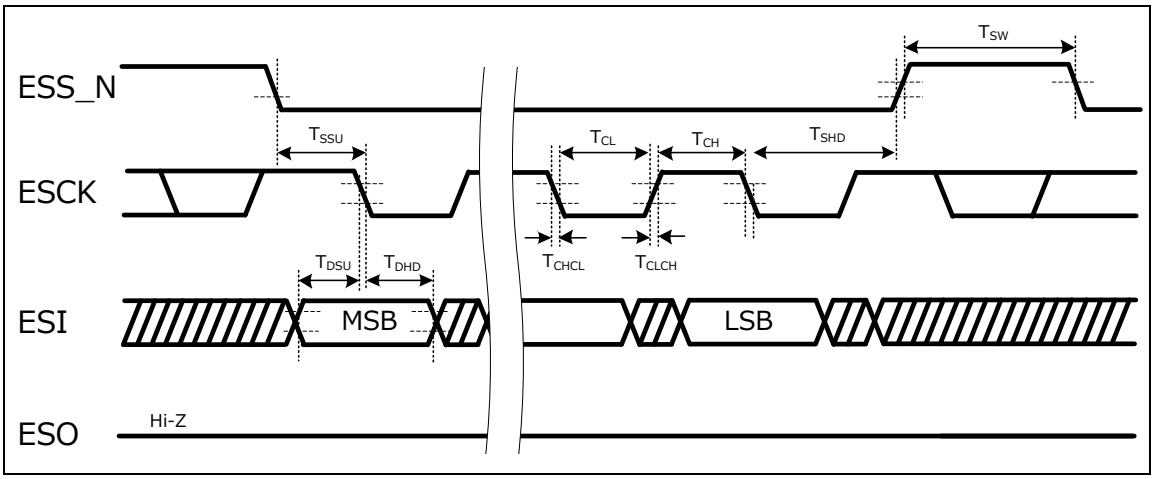
I_{OH} = −2 mA, I_{OL} = +2 mA

- **Timing Diagram for Serial Input Operations**

Mode 0, 3

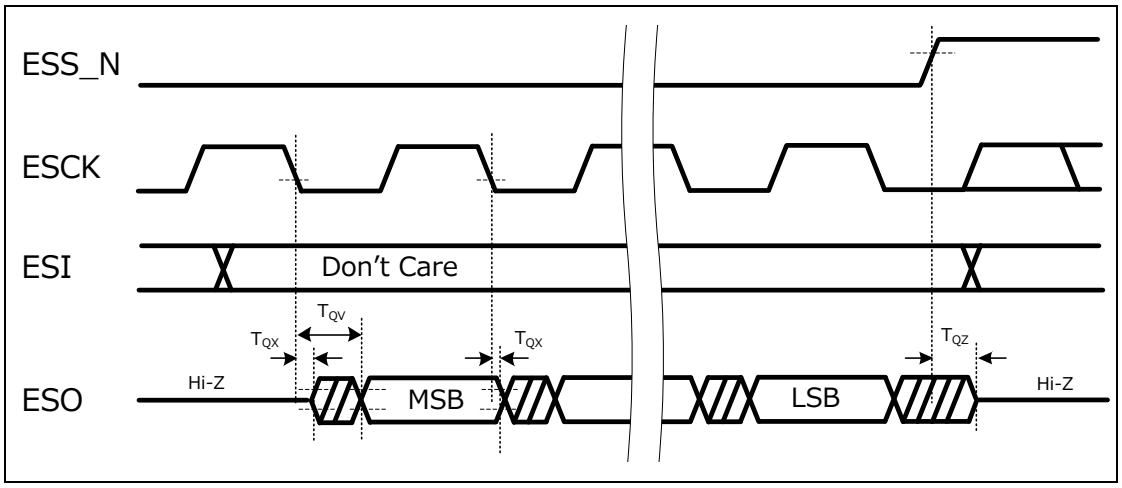


Mode 1, 2

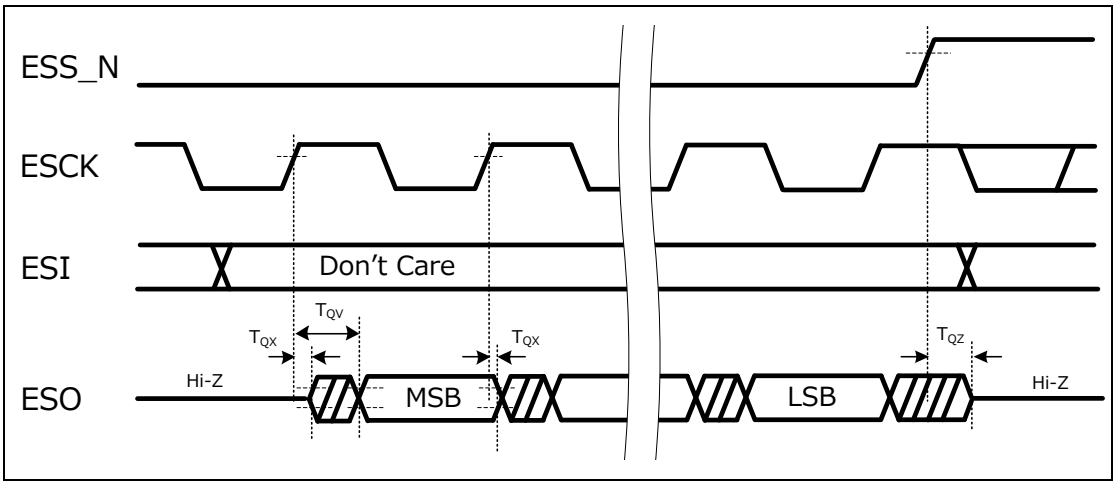


- **Timing Diagram for Serial Output Operations**

Mode 0, 3

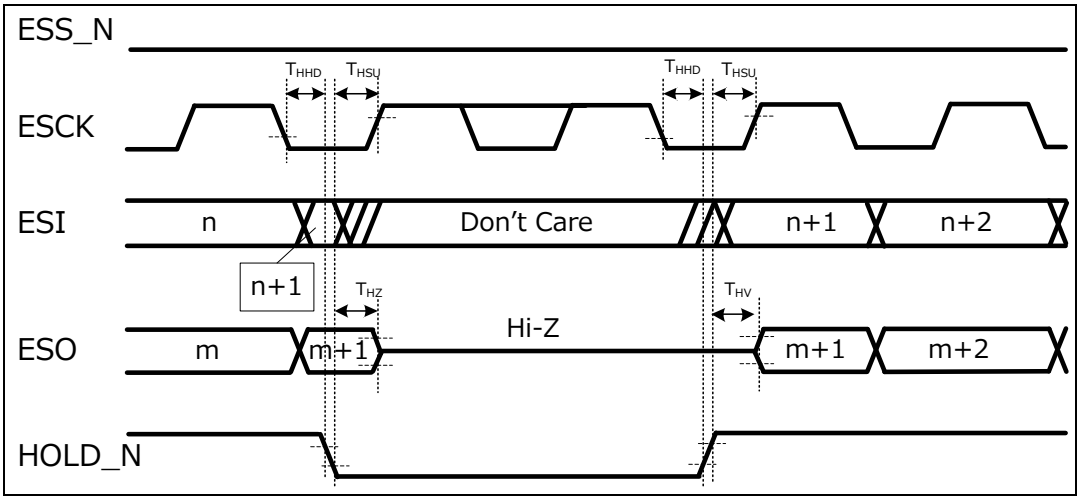


Mode1, 2

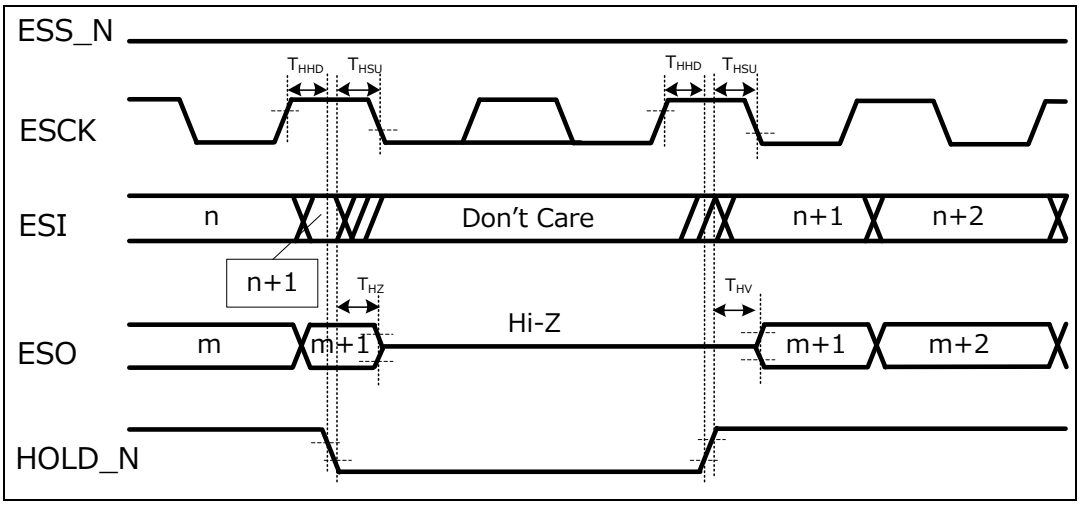


- **Timing Diagram for Hold Operations**

Mode 0, 3



Mode 1, 2



• Digital Audio Interface Timing

Followings are the conditions assumed for the specified values.

Input logic voltage levels : V_{IH} = 0.80 × IOVDD2, V_{IL}=0.20 × IOVDD2

Input, output timing reference levels : V_{IH} = 0.70 × IOVDD2, V_{IL}= 0.30 × IOVDD2

V_{OH} =0.70 × IOVDD2, V_{OL}=0.30 × IOVDD2

i) Common to Master Mode and Slave Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
SDI input setup time	T_{SDIS}	65			ns
SDI input hold time	T_{SDIH}	65			ns
SDO output delay time					
(Of the first bit after LRCK toggles) (*4)	T_{DSDOL}	0		65	ns
(Other than above) (*4)	T_{DSDOB}	0		65	ns

ii) Master Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
BCLK output frequency (*2)(*3)	1 / T_{BCLKW}		64$fs_{_DA}$ 48$fs_{_DA}$ 32$fs_{_DA}$ (*1)		kHz
BCLK output “H” time	T_{BCLKHW}	120			ns
BCLK output “L” time	T_{BCLKLW}	120			ns
BCLK output rise / fall time	T_{BCLKRF}			20	ns
LRCK output frequency (*3)	1 / T_{LRCKW}		$fs_{\_DA}$(*1)		kHz
LRCK output delay time	T_{DLRCK}	-50		50	ns
LRCK output rise / fall time	T_{LRCKRF}			20	ns

iii) Slave Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
BCLK input frequency	1 / T_{BCLKW}		64$fs_{_DA}$ 48$fs_{_DA}$ 32$fs_{_DA}$ (*1)		kHz
BCLK input “H” time	T_{BCLKHW}	120			ns
BCLK input “L” time	T_{BCLKLW}	120			ns
BCLK input rise / fall time	T_{BCLKRF}			20	ns
LRCK input frequency	1 / T_{LRCKW}		$fs_{\_DA}$ (*1)		kHz
LRCK input setup time	T_{LRCKS}	65			ns
LRCK input hold time	T_{LRCKH}	65			ns
LRCK input rise / fall time	T_{LRCKRF}			20	ns

[Conditions] With the Recommended Operating Conditions, and capacitive load of 30 pF

I_{OH} = −1.0 mA, I_{OL} = +1.0 mA (IOVDD ≥ 2.20 V)

I_{OH} = −0.2 mA, I_{OL} = +0.2 mA (IOVDD < 2.20 V)

(*1) $fs_{\_DA}$ is the sampling frequency of the digital audio interface.

(*2) BCLK outputs have jitters from logic operations.

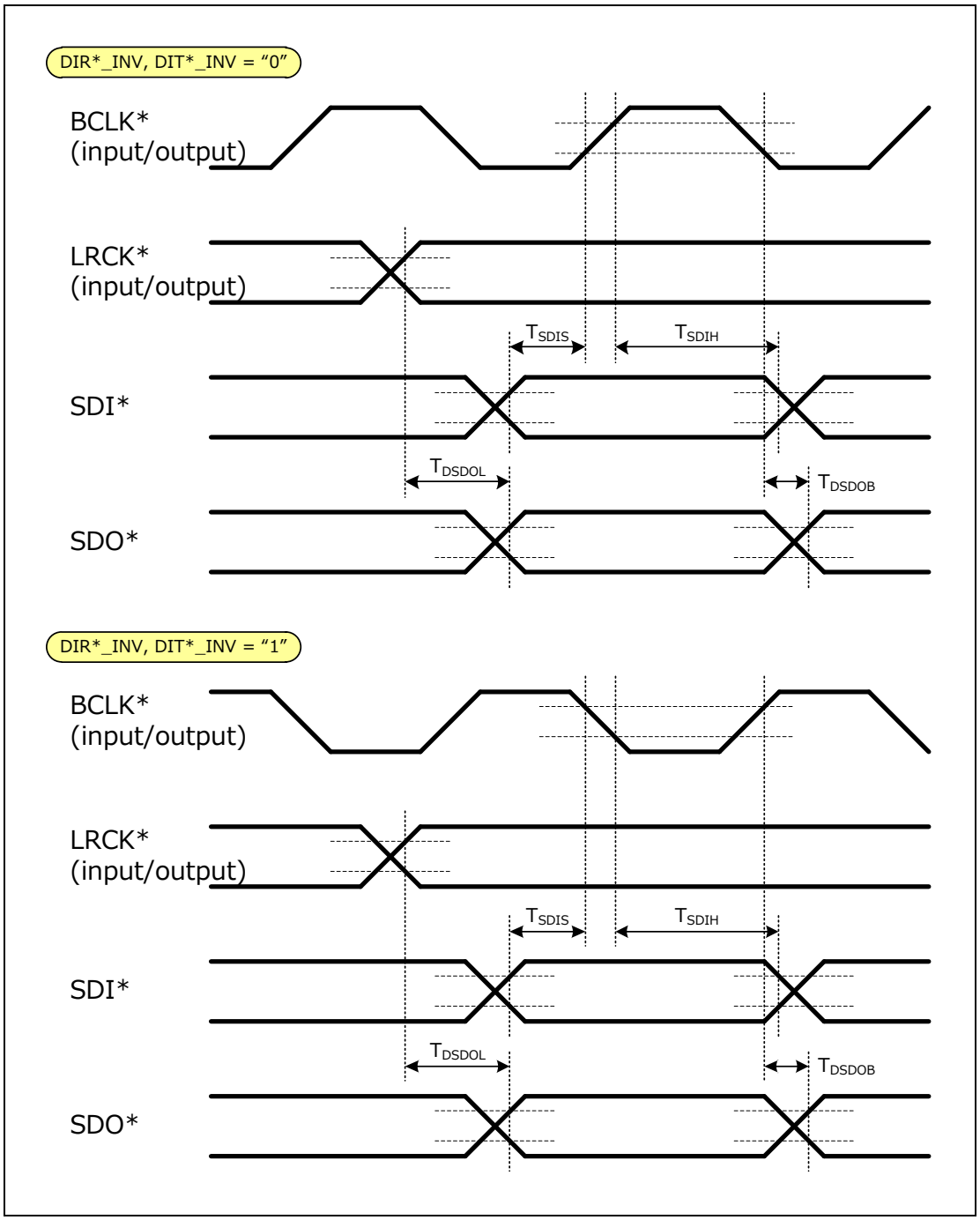
(*3) Clocks may not be at the exact frequency for particular CLKI frequency and PLL settings.

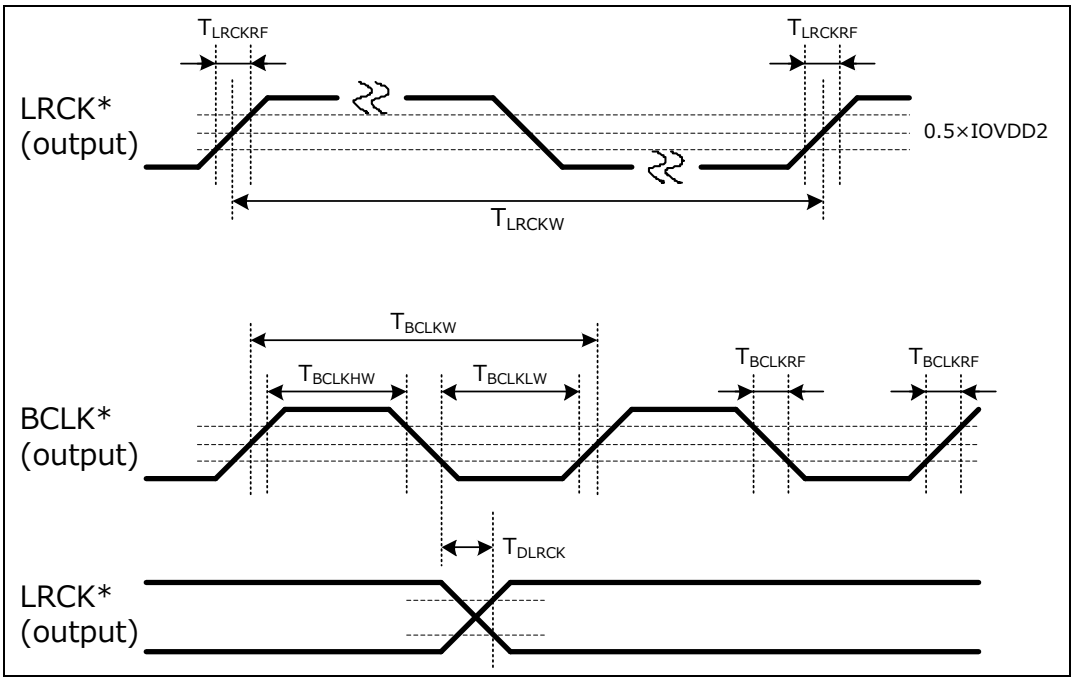
(*4) The value for *(Other than above)* case apply all the time for I^2S format timing.

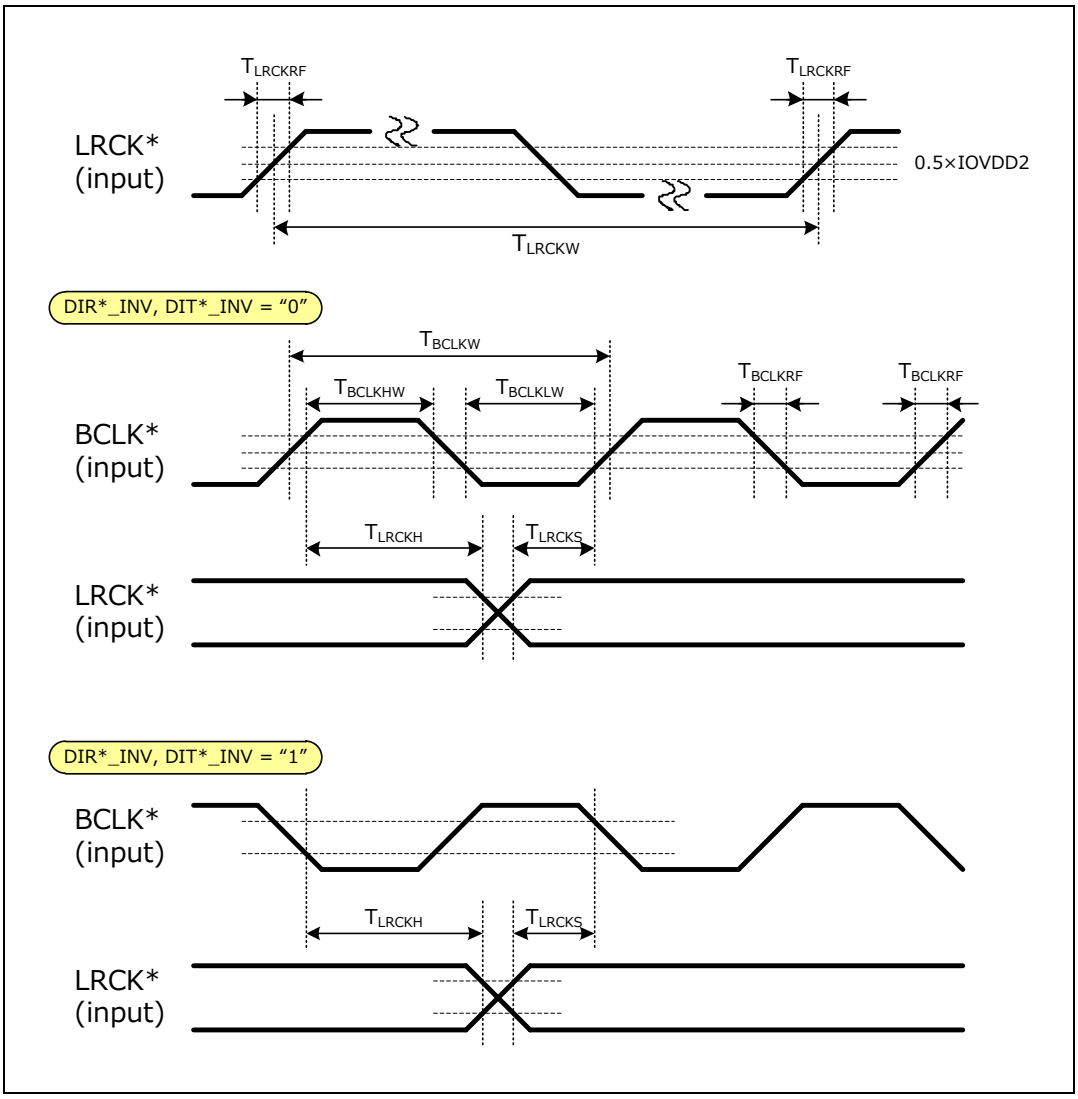
Incoming (LRCK) Frequency Range Limitation

As a slave mode device, the input frequency of LRCK has limited range.

Using LRCK outside this range may result in failed playbacks.




TLRCKRF
TLRCKRF
LRCK*
(output)
0.5×IOVDD2
TLRCKW
TBCLKW
TBCLKHW
TBCLKLW
TBCLKRF
TBCLKRF
BCLK*
(output)
TDLRCK
LRCK*
(output)

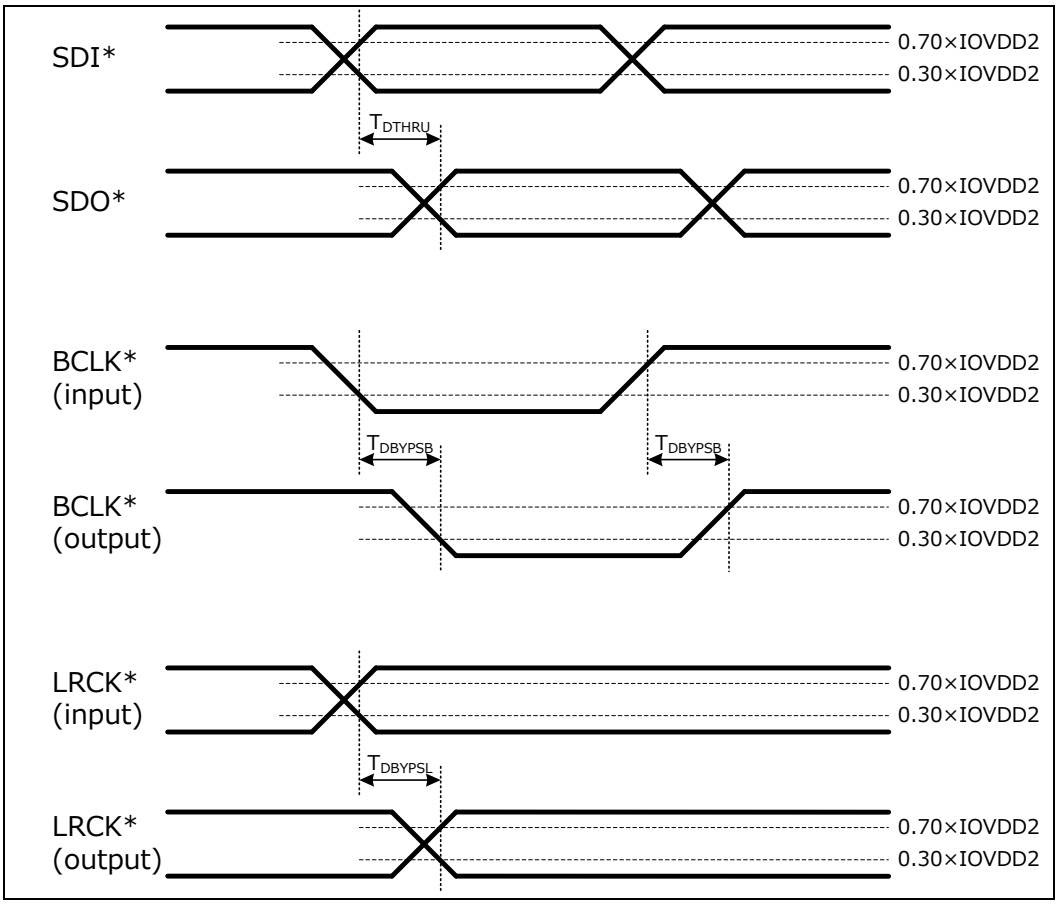

TLRCKRF
TLRCKRF
LRCK*
(input)
0.5×IOVDD2
TLRCKW
DIR*_INV, DIT*_INV = "0"
TBCLKW
TBCLKHW
TBCLKLW
TBCLKRF
TBCLKRF
BCLK*
(input)
TLRCKH
TLRCKS
LRCK*
(input)
DIR*_INV, DIT*_INV = "1"
BCLK*
(input)
TLRCKH
TLRCKS
LRCK*
(input)

iv) Transit Time in Bypass Mode

These are the transit time when the interface is in bypass mode.

Parameter	Symbol	Min.	Typ.	Max.	Unit
SDI→SDO output delay time	T_{DTHRU}			50	ns
BCLK→BCLK delay time	T_{DBYPSB}			50	ns
LRCK→LRCK delay time	T_{DBYPSL}			50	ns

[Conditions] With the Recommended Operating Conditions, and apacitive load of 30 pF



• PCM Interface Timing

Followings are the conditions assumed for the specified values.

Input logic voltage levels : V_{IH} = 0.80 × IOVDD2, V_{IL}=0.20 × IOVDD2

Input, output timing reference levels : V_{IH} = 0.70 × IOVDD2, V_{IL}= 0.30 × IOVDD2

V_{OH} =0.70 × IOVDD2, V_{OL}=0.30 × IOVDD2

i) Master Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
SDI input setup time	T_{SDIS}	65			ns
SDI input hold time	T_{SDIH}	65			ns
BCLK output frequency (*2)(*3)	1 / T_{BCLKW}		64$fs_{_DA}$ 48$fs_{_DA}$ 32$fs_{_DA}$ 24$fs_{_DA}$ 16$fs_{_DA}$ (*1)		kHz
BCLK output “H” time	T_{BCLKHW}	450			ns
BCLK output “L” time	T_{BCLKLW}	450			ns
BCLK output rise / fall time	T_{BCLKRF}			20	ns
LRCK output frequency	1 / T_{LRCKW}		8, 16		kHz
LRCK output delay time	T_{DLRCK}	-50		50	ns
LRCK output rise / fall time	T_{LRCKRF}			20	ns
SDO output delay time (First bit in Slot 0) (Other than above)	 T_{D0SDO} T_{D1SDO}	 0 0		 80 80	ns
SDO High-impedance transition time	T_{DZSDO}	0		60	ns

[Conditions] With the Recommended Operating Conditions, and capacitive load of 30 pF

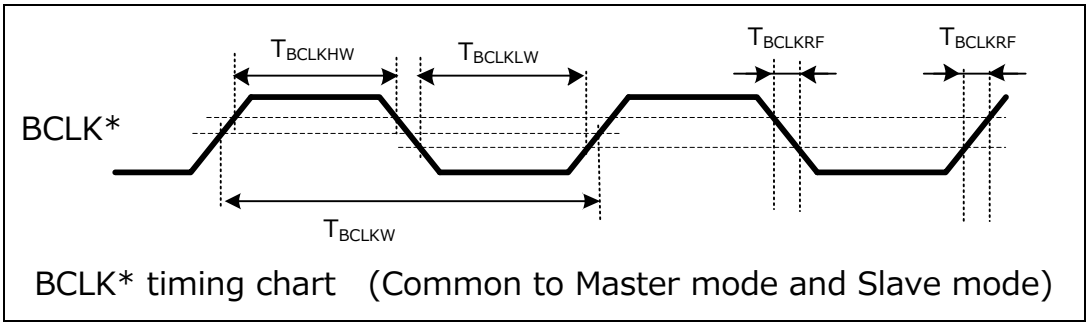
I_{OH} = −1.0 mA, I_{OL} = +1.0 mA (IOVDD ≥ 2.20V)

I_{OH} = −0.2 mA, I_{OL} = +0.2 mA (IOVDD < 2.20V)

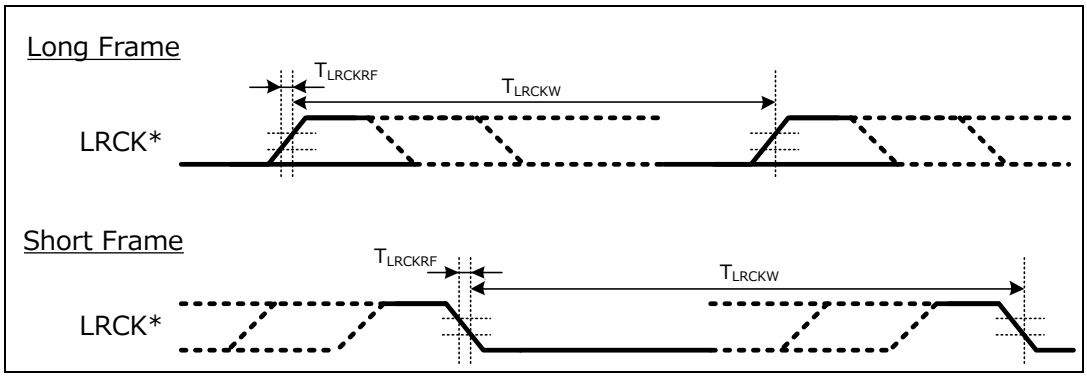
(*1) $fs_{\_DA}$ is the sampling frequency of the PCM interface.

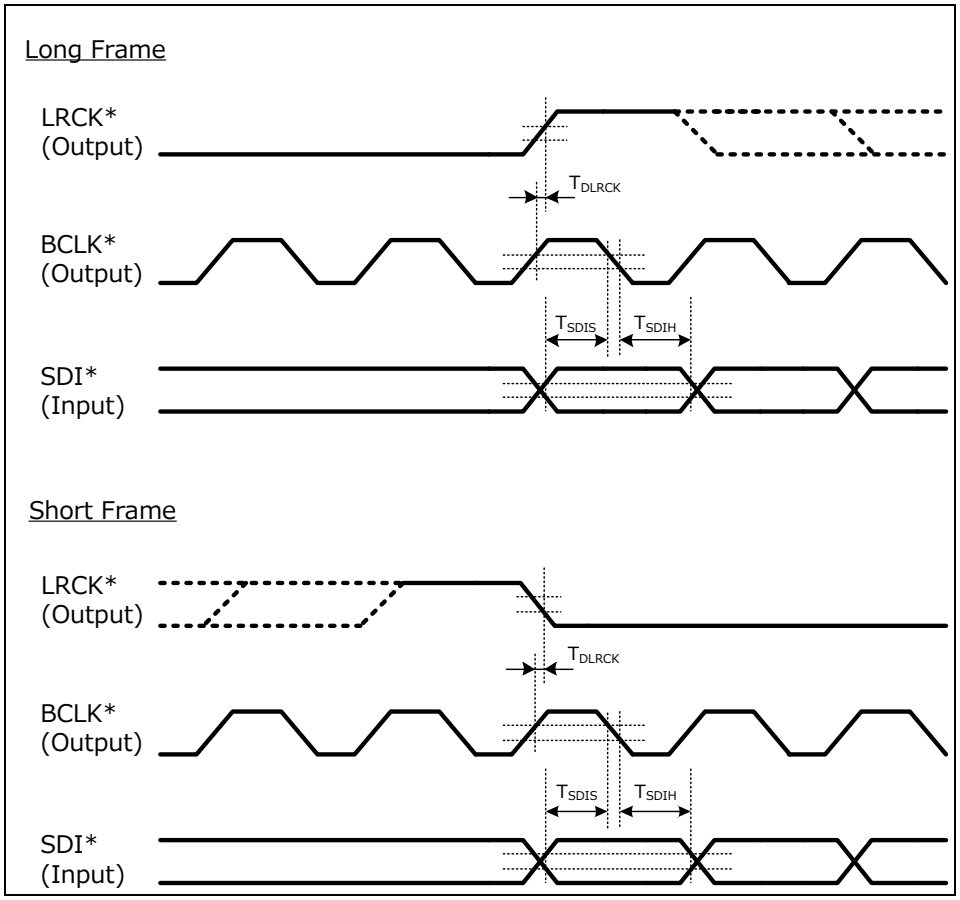
(*2) BCLK outputs have jitters from logical operations.

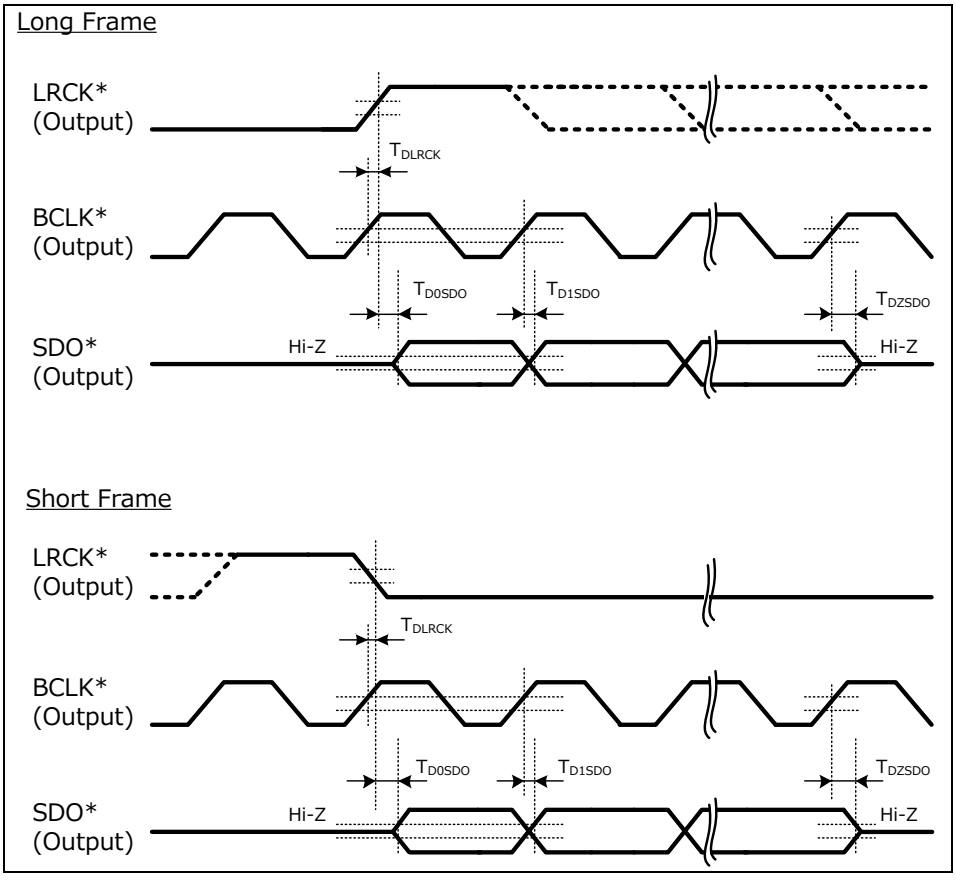
(*3) Clocks may not be at the exact frequency for particular CLKI frequency and PLL settings.



BCLK* timing chart (Common to Master mode and Slave mode)




Long Frame
LRCK*
(Output)
TDLRCK
BCLK*
(Output)
TSDIS
TSDIH
SDI*
(Input)
Short Frame
LRCK*
(Output)
TDLRCK
BCLK*
(Output)
TSDIS
TSDIH
SDI*
(Input)


Long Frame
LRCK*
(Output)
TDLRCK
BCLK*
(Output)
TD0SDO
TD1SDO
TDZSDO
SDO*
(Output)
Hi-Z
Hi-Z
Short Frame
LRCK*
(Output)
TDLRCK
BCLK*
(Output)
TD0SDO
TD1SDO
TDZSDO
SDO*
(Output)
Hi-Z
Hi-Z

ii) Slave Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
SDI input setup time	T_{SDIS}	65			ns
SDI input hold time	T_{SDIH}	65			ns
BCLK input frequency (*2)	$1 / T_{BCLKW}$		16$fs_{_DA}$ to 256$fs_{_DA}$ (*1)		kHz
BCLK input "H" time	T_{BCLKHW}	90			ns
BCLK input "L" time	T_{BCLKLW}	90			ns
BCLK input rise / fall time	T_{BCLKRF}			20	ns
LRCK input frequency	$1 / T_{LRCKW}$		8, 16		kHz
LRCK input "H" time	T_{LRCKHW}	2			BCLK cycle
LRCK input "L" time	T_{LRCKLW}	2			BCLK cycle
LRCK input setup time	T_{LRCKS}	65			ns
LRCK input hold time	T_{LRCKH}	65			ns
LRCK input rise / fall time	T_{LRCKRF}			20	ns
SDO input delay time					
(First bit of Slot 0)	T_{D0SDO}	0		80	ns
(Other than above)	T_{D1SDO}	0		80	
SDO High-impedance transition time	T_{DZSDO}	0		60	ns

[Conditions] With the Recommended Operating Conditions, and capacitive load of 30 pF

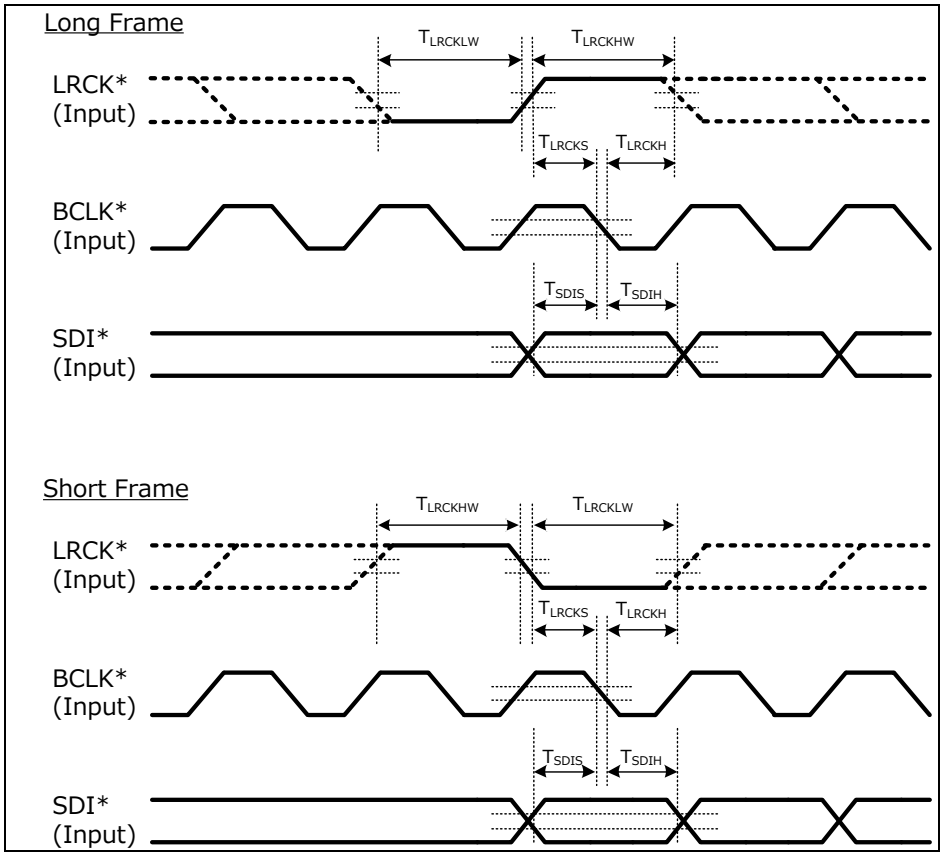
(*1) $fs_{\_DA}$ is the sampling frequency of the PCM interface.

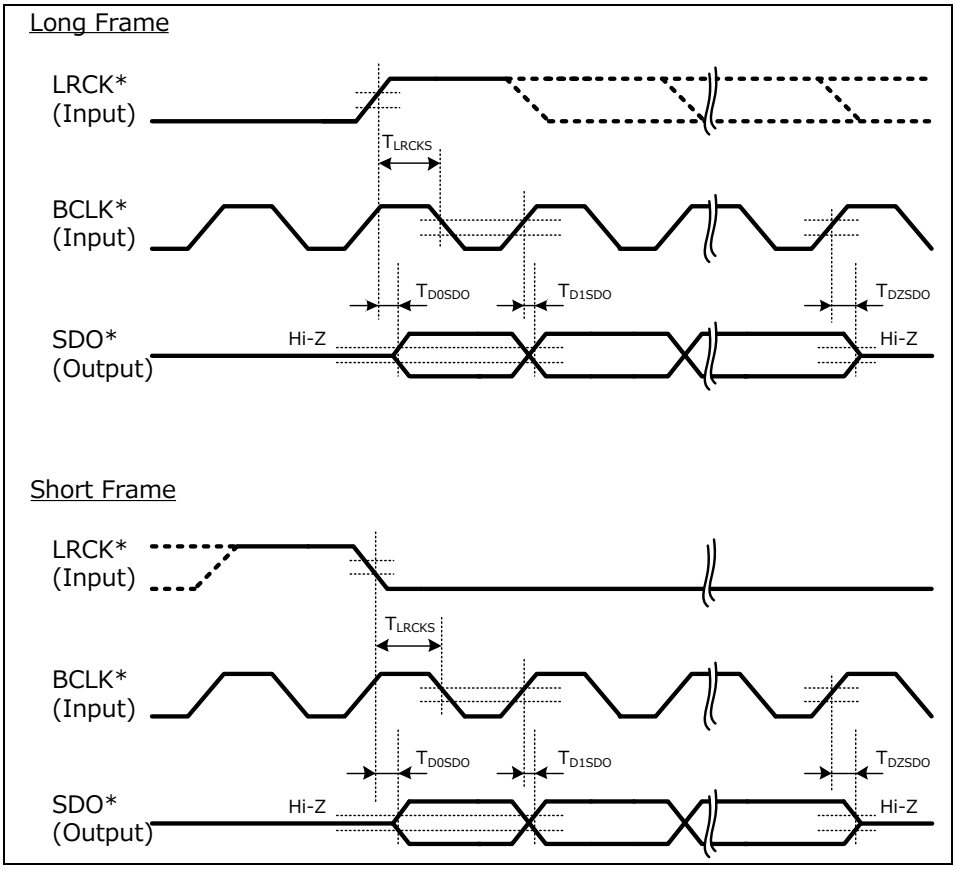
(*2) The (*3) Clocks may not be at the exact frequency for particular CLKI frequency and PLL settings.

Incoming (LRCK) Frequency Range Limitation

As a slave mode device, the input frequency of LRCK has limited range.

Using LRCK outside this range may result in failed playbacks.


Long Frame
TLRCKLW
TLRCKHW
LRCK*
(Input)
TLRCKS
TLRCKH
BCLK*
(Input)
TSDIS
TSDIH
SDI*
(Input)
Short Frame
TLRCKHW
TLRCKLW
LRCK*
(Input)
TLRCKS
TLRCKH
BCLK*
(Input)
TSDIS
TSDIH
SDI*
(Input)


Long Frame
LRCK*
(Input)
TLRCKS
BCLK*
(Input)
TD0SDO
TD1SDO
TDZSDO
SDO*
(Output)
Hi-Z
Hi-Z
Short Frame
LRCK*
(Input)
TLRCKS
BCLK*
(Input)
TD0SDO
TD1SDO
TDZSDO
SDO*
(Output)
Hi-Z
Hi-Z

• GPIO

Followings are the conditions assumed for the specified values.

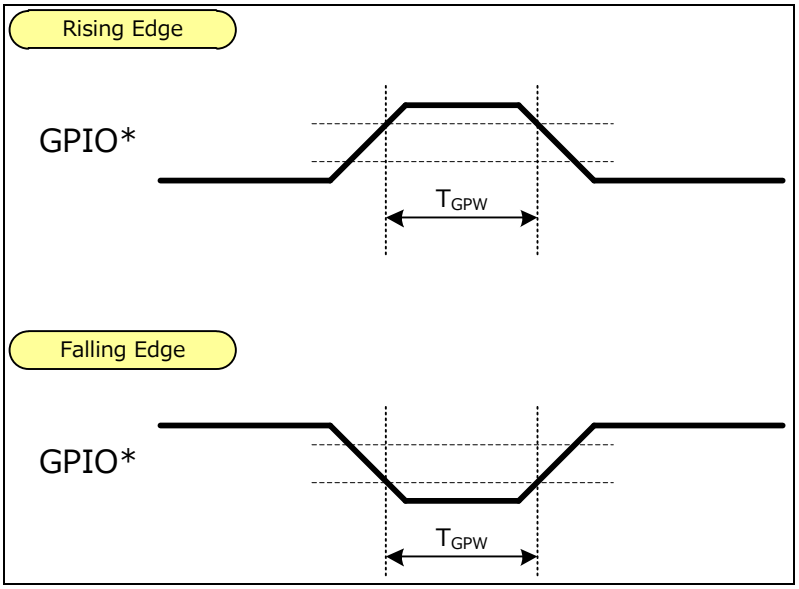
Input logic voltage levels : V_{IH} = 0.80 × IOVDD2, V_{IL}=0.20 × IOVDD2

Input, output timing reference levels : V_{IH} = 0.70 × IOVDD2, V_{IL}= 0.30 × IOVDD2

V_{OH} =0.70 × IOVDD2, V_{OL}=0.30 × IOVDD2

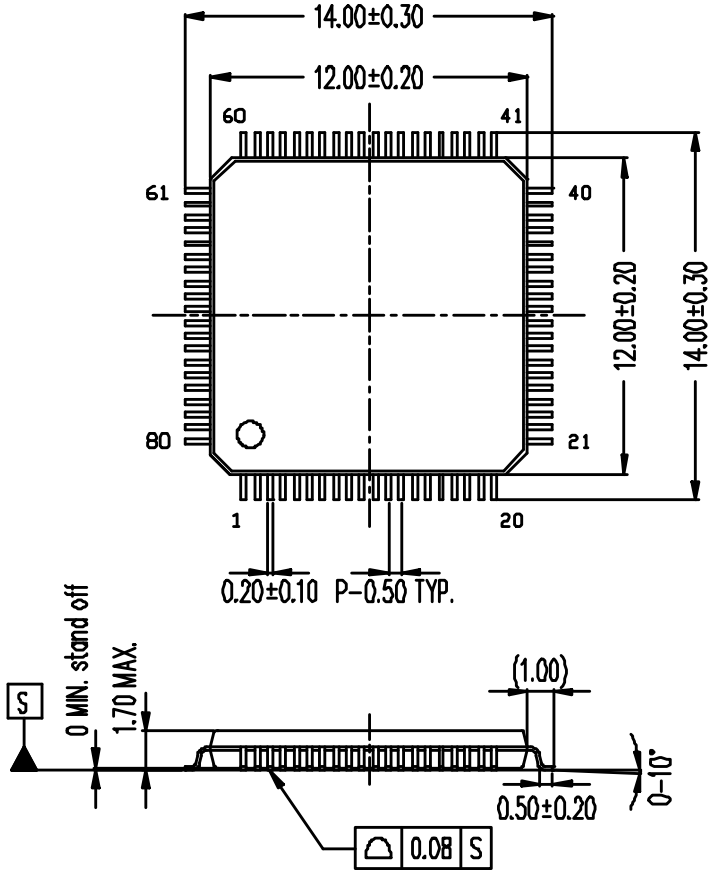
Parameter	Symbol	Min.	Typ.	Max.	Unit
Pulse width (Interrupt)	T_{GPW}	80			ns

[Conditions] With the Recommended Operating Conditions.



■ Package Information

U-PK80SP1-01-1



端子厚さ：0.17±0.05
Lead Thickness

カッコ内の寸法値は参考値とします。
The value parenthesized is not specified.

モールド外形寸法はバリを含みません。
Plastic body dimensions do not include burr of resin.

単位 (UNIT)：mm (millimeters)

注） 1. 表面実装LSIは、保管条件、および、半田付けについての特別な配慮が必要です。
2. 組立工場により、寸法や形状などが異なる場合があります。
詳しくはヤマハ代理店までお問い合わせください。

Note: 1. Special attention needs to be paid to the storage conditions and soldering method of the surface mount IC.
2. Dimension, form, etc. may differ depending on assembly plants.
For details, please contact your local Yamaha agent.

PRECAUTIONS AND INSTRUCTIONS FOR SAFETY

	WARNING
Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings. Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causing breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins. In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, such as the consequences of unusual speaker output due to a malfunction or failure. A speaker dissipates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat dissipation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoking or ignition of the speaker even if it is used within the rated input value.

	CAUTION
Prohibited	Do not use Yamaha products in close proximity to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of the designer to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (the ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as using overcurrent protection circuits to control the amount of current during operation and to shut off on failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high-temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the protection circuit kicks in.
Instructions	Use a robust power supply. The use of an unrobust power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the considerations of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation. Therefore, please take care not to touch an operating device directly.

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AGENT

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