Solid State Music

SSM2000
SSM2020
Application Note

LINEAR-ANTILOG VOLTAGE CONTROLLED AMPLIFIERS

The SSM 2000 and 2020 are dual two quadrant multipliers designed to be used with op amps in a wide variety of precision audio frequency applications. Each channel of the two devices has differential signal inputs, current output and its own control circuit which allows the designer an independent choice of linear or exponential control characteristics and scale factor. Both parts are fully temperature compensated and have excellent distortion and signal to noise figures.

In order to show as many applications of these versatile circuits as possible in this short space, control circuits are presented in a separate section and are referred to in the application section.

CONTROL CIRCUITS SSM 2000

To produce a linear control of amplification in the SSM2000, a linear voltage to current converter is used to supply an output control current from an input voltage. The circuit in Fig. 1A is used for a positive control voltage ($V_C/R_C = I_C$), and Fig. 1B for a negative voltage ($-V_C/R_C = I_C$). The resistor in these circuits should be chosen so that the maximum desired input voltage will produce an output current of 1mA or less. The Fig. 1A circuit has the advantage of higher input impedance and in Fig. 1B a larger control voltage can be used without running into the bias voltage on the control pin (V_{CC} −4V). The circuit in Fig. 1c will gang the gain of both halves of the I.C. to the same control voltage, without using two op amps. The 3.3K resistors force a match in the control currents in both VCA's and also offer current limiting. This approach will closely match the gain of the two channels as the voltage drop across the matching resistors is 50mV or greater.

ANTILOG CONTROL GRAPH

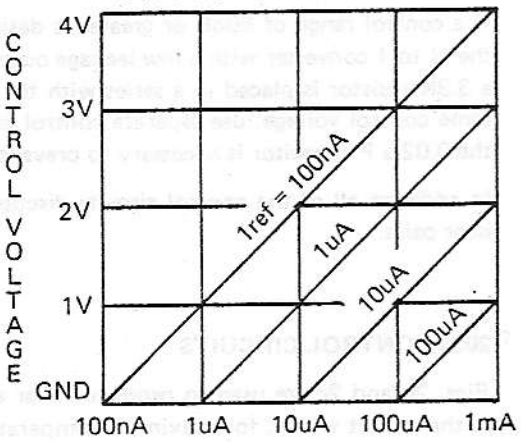


FIGURE 1a

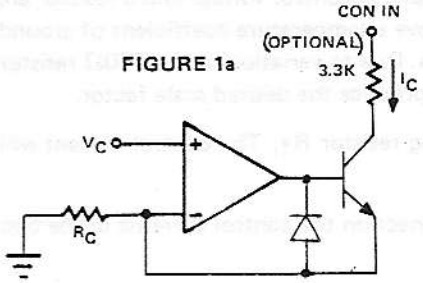


FIGURE 1b

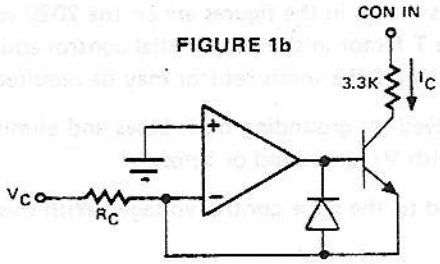
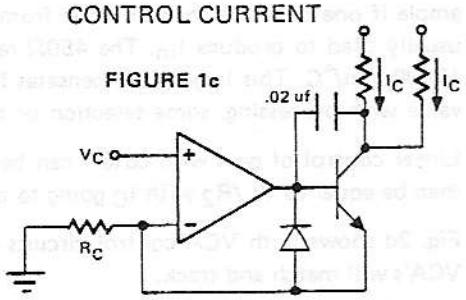


FIGURE 1c



Antilog control of gain is achieved by the exponential voltage to current converter in Fig. 1d. The graph shows the Antilog I_C to V_C relationship at various reference currents. As can be seen from the graph, the range of control is determined by the reference current which is set up by the circuits in Figs. 1e or 1f; 80dB for I_{REF} = 100nA etc. The scale factor, 1 decade per volt, is determined by the attenuator which in this case gives 60 mV at the op amp non-inverting input for 1 volt at the control input. In the more general case:

$$\ln(I_C/I_{REF}) = R_1 \, Vin/(R_1 + R_2) \, V_T \qquad V_T = kT/q$$

FIGURE 1d

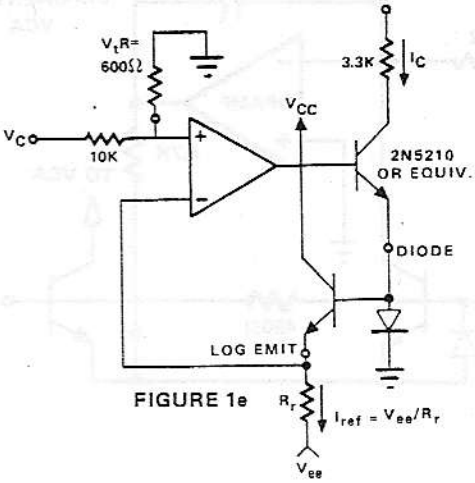


FIGURE 1e

FIGURE 1f

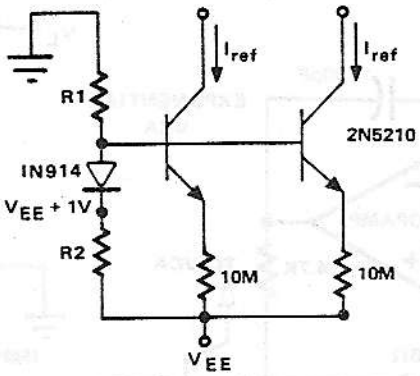
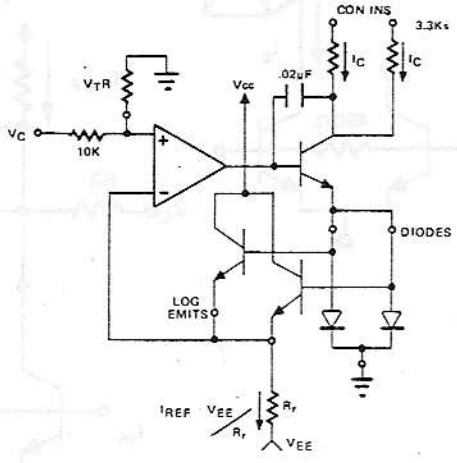


FIGURE 1g



Solid State Music, 2102A Walsh Ave., Santa Clara, CA 95050
(408) 246-2707

As one can see this expression is temperature sensitive. This effect can be largely cancelled if the V_T resistor provided on the chip is used for R_1. With this resistor an 80dB control range can be used with a ±10% error due to temperature over the span from 10°C to 45°C. This worst case error will occur for the largest control current in the range. An ordinary resistor can be used as R_1 for room temperature applications (25°C ± 10°C) with only a 10% error if the control range is restricted to 40dB. (100 to 1). An ideal temperature compensating resistor would have a temperature coefficient of 3300ppm/°C. If extremely precise V_T temperature compensation is required in the antilog control mode, a Tel Labs Type Q81 resistor or equivalent can be used in place of the on chip V_T resistor. Another alternative is to use a Fairchild μA726 Temperature Controlled Differential pair in place of the on chip logging elements. In this case, no V_T resistor is required.

If a control range of 60dB or greater is desired, a low input bias op amp such as the LF356 or the Teledyne 844 should be used in the V to I converter with a low leakage output transistor such as a 2N5210 or a 2N930. As with the linear inverting control circuit, a 3.3K resistor is placed in a series with the collector of the output transistor for current limiting. To gang both amplifiers to the same control voltage, use separate control circuits or the circuit in Fig. g which is designed to provide a 20dB gain change per volt; the 0.02μ F capacitor is necessary to prevent oscillation.

In addition all of the control circuits discussed below for the 2020 can be used with the 2000 if one adds external matched transistor pairs.

2020 CONTROL CIRCUITS

Figs. 2b and 2c are used to produce linear and, or exponential voltage control of gain. Resistor R_1 establishes a reference current in the circuit which, for maximum temperature stability, should be chosen at the logarithmic center of the control range. For example if one desires a control range from 500μA to 50nA the reference current would be 5μA. A control voltage and a resistor are usually used to produce I_{in}. The 450Ω resistors shown in the figures are on the 2020 and have a temperature coefficient of around +2000ppm/°C. This largely compensates for the T factor in the exponential control equation. Due to variation of the 450Ω resistor value with processing, some selection or trimming of the input resistor may be required to produce the desired scale factor.

Linear control of gain with cutoff can be achieved by grounding both bases and eliminating resistor R_1. The control current will then be equal to V_L/R_2 with I_C going to zero with V_L at ground or below.

Fig. 2d shows both VCA control circuits ganged to the same control voltages. With this connection the control currents in the two VCA's will match and track.

Figs. 2i and 2j show two circuits for producing a control current that is proportional to the amplitude of an AC input signal. Fig. 2i is an AC to DC converter that has equal attack and decay times. Fig. 2j is a peak detector that has fast attack and slow delay. Both circuits are useful in compander and AGC applications. Inexpensive dual op amps such as the 1458 can be used without trimming for good results over a 50dB input range.

FIGURE 2a

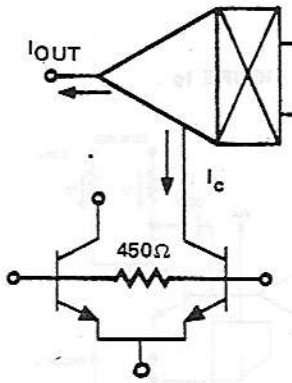


FIGURE 2b

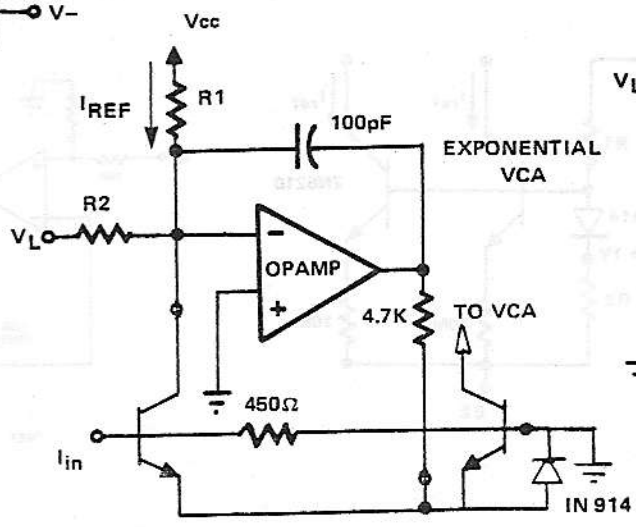


FIGURE 2c

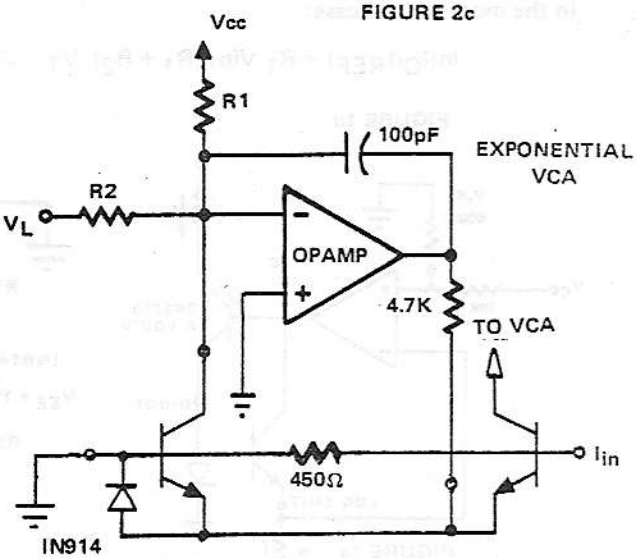


FIGURE 2d

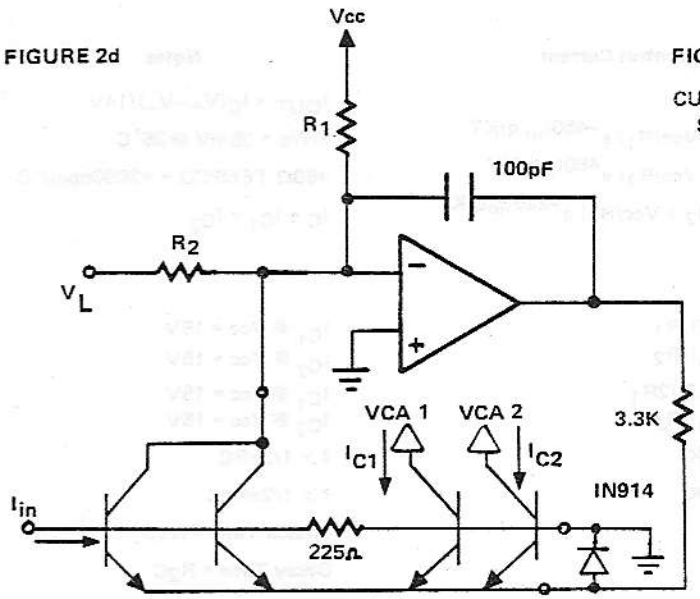


FIGURE 2e
CURRENT SINK

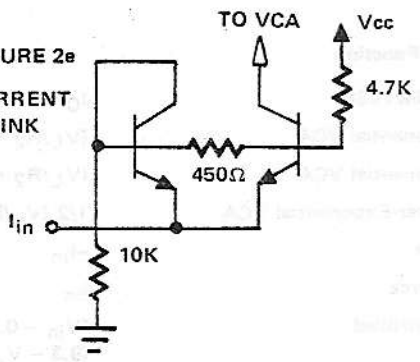


FIGURE 2f
CURRENT SOURCE

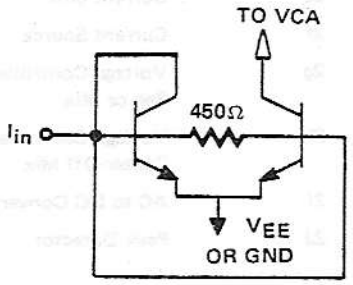


FIGURE 2g
VC PAN OR MIX

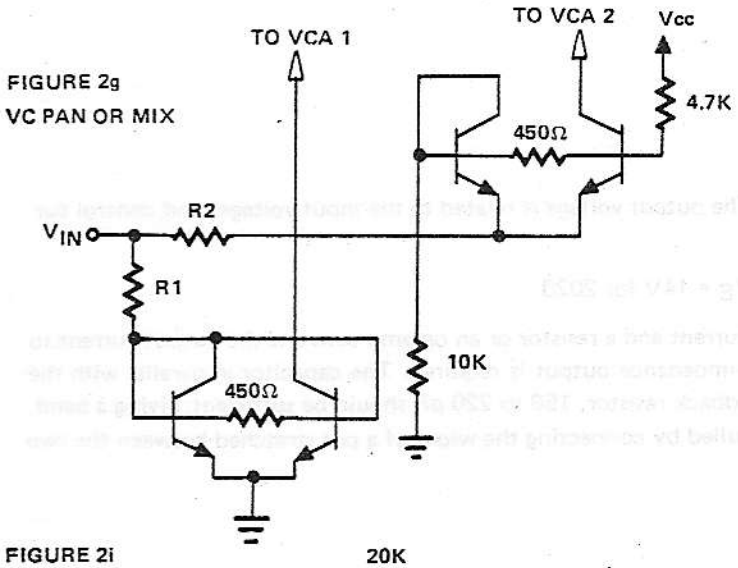


FIGURE 2h
VC CENTER-OFF MIX

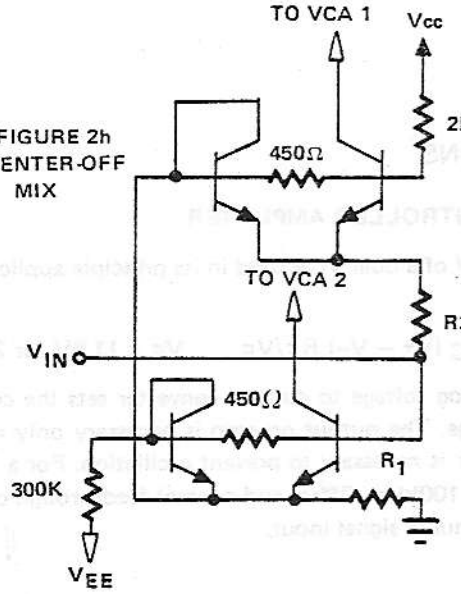


FIGURE 2i

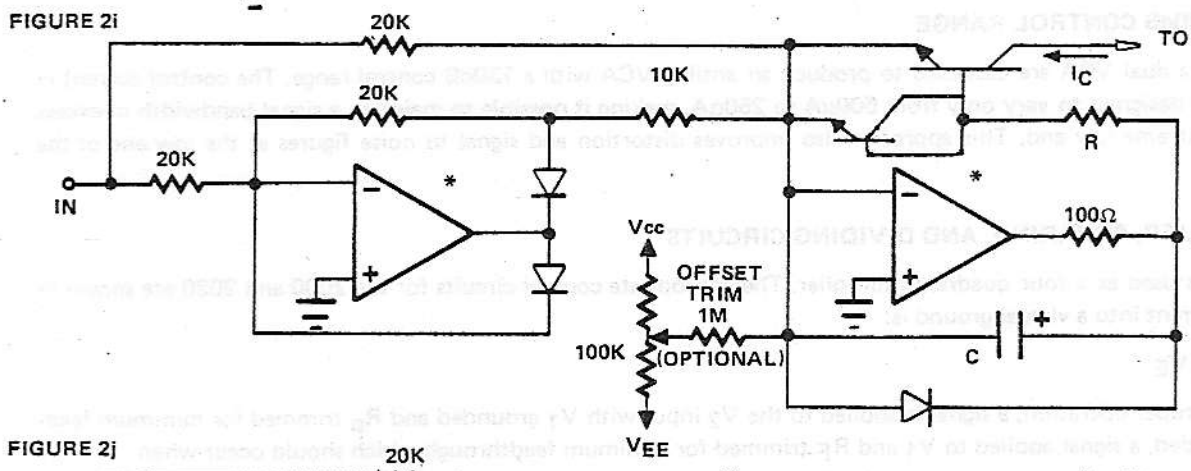
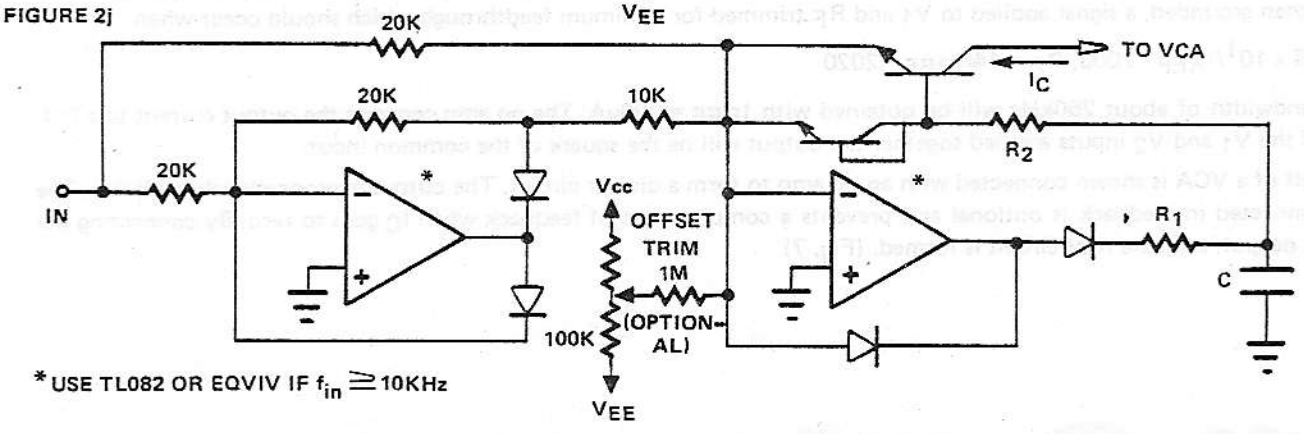


FIGURE 2j



*USE TL082 OR EQVIV IF $f_{in} \geq 10KHz$

TABLE 1. 2020 DESIGN EQUATIONS

Figure	Function	Control Current	Notes
2a	One Side SSM 2020	I_C	$I_{OUT} = I_C(V_+ - V_-)/14V$
2b	Linear-Exponential VCA	$(V_L/R_2 + Vcc/R_1)\, e^{-450 I_{in}\, q/KT}$	KT/q = 25mV @ 25°C
2c	Linear-Exponential VCA	$(V_L/R_2 + Vcc/R_1)\, e^{450 I_{in} q/KT}$	450Ω TEMPCO = +2000ppm/°C
2d	Ganged Linear-Exponential VCA	$1/2\,(V_L/R_2 + Vcc/R_1)\, e^{-225 I_{in} q/KT}$	$I_C = I_{C_1} = I_{C_2}$
2e	Current Sink	$-I_{in}$	
2f	Current Source	I_{in}	
2g	Voltage Controlled Pan or Mix	$(V_{in} - 0.7)/R_1$ $(9.3 - V_{in})/R_2$	I_{C_1} @ Vcc = 15V I_{C_2} @ Vcc = 15V
2h	Voltage Controlled Center-Off Mix	$3(V_{in} - 5.7)/2R_1$ $(4.3 - V_{in})/R_2$	I_{C_1} @ Vcc = 15V I_{C_2} @ Vcc = 15V
2I	AC to DC Converter	Vpp in/40K	$f > 1/2\pi RC$
2J	Peak Detector	Vpp in/40K	$f > 1/2\pi R_2 C$ Attack Time = R_1C Decay Time = R_2C

APPLICATIONS

VOLTAGE CONTROLLED AMPLIFIER

Fig. 3 shows half of a dual VCA used in its principle application. The output voltage is related to the input voltages and control current by:

$$V_{OUT} = I_C\,(V+ - V-)\,R_F/V_E \qquad V_E = 11.8V \text{ for 2000, } V_E = 14V \text{ for 2020}$$

A linear or antilog voltage to current converter sets the control current and a resistor or an op amp converts the output current to an output voltage. The output op amp is necessary only if a low-impedance output is required. The capacitor in parallel with the feedback resistor is necessary to prevent oscillation. For a 10K feedback resistor, 150 to 220 pF should be sufficient, giving a band width of about 100kHz. Offset and control feedthrough can be nulled by connecting the wiper of a pot stretched between the two supplies to an unused signal input.

ANTILOG VCA WITH 130dB CONTROL RANGE

In Fig. 4, both halves of a dual VCA are cascaded to produce an antilog VCA with a 130dB control range. The control current in each half of the device is designed to vary only from 500μA to 250nA, making it possible to maintain a signal bandwidth in excess of 50kHz down to the extreme low end. This approach also improves distortion and signal to noise figures at the low end of the control range.

4 QUADRANT MULTIPLIER, SQUARING, AND DIVIDING CIRCUITS

In Fig. 5 half of a VCA is used as a four quadrant multiplier. The appropriate control circuits for the 2000 and 2020 are shown in the figure. The output current into a virtual ground is:

$$I_{OUT} = -V_1 V_2/R_C\, V_E$$

To adjust the circuit for proper operation, a signal is applied to the V_2 input with V_1 grounded and R_p trimmed for minimum feedthrough. V_2 is then grounded, a signal applied to V_1 and R_F trimmed for minimum feedthrough which should occur when:

$$R_F = 1.18 \times 10^1/I_{REF} \quad 2000, \; R_F = 14/I_{REF} \quad 2020$$

A maximum bandwidth of about 250kHz will be obtained with I_{REF} = 200μA. The op amp converts the output current to a buffered voltage. If the V_1 and V_2 inputs are tied together the output will be the square of the common input.

In Fig. 6 one half of a VCA is shown connected with an op amp to form a divider circuit. The output is proportional to V_1/V_2. The 22M resistor connected in feedback is optional and prevents a complete loss of feedback when I_C goes to zero. By connecting the V_2 input to the output, a square root circuit is formed. (Fig. 7)

FIGURE 3

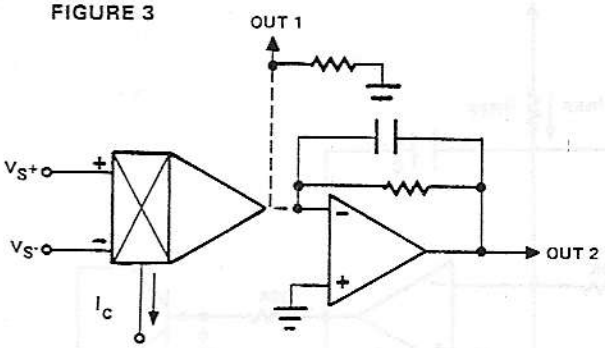


FIGURE 4

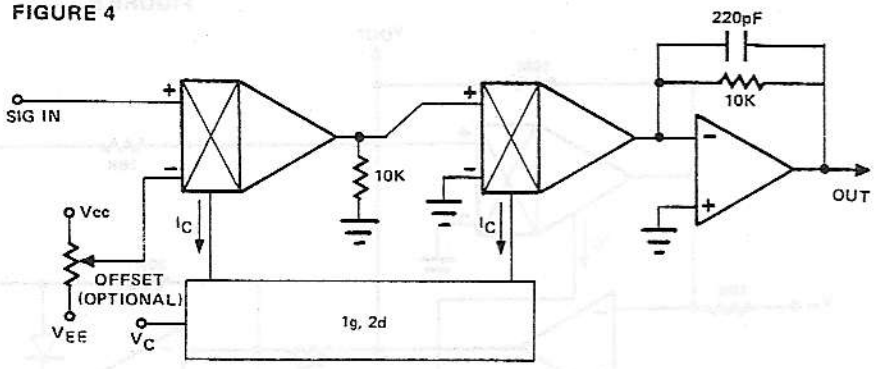


FIGURE 5

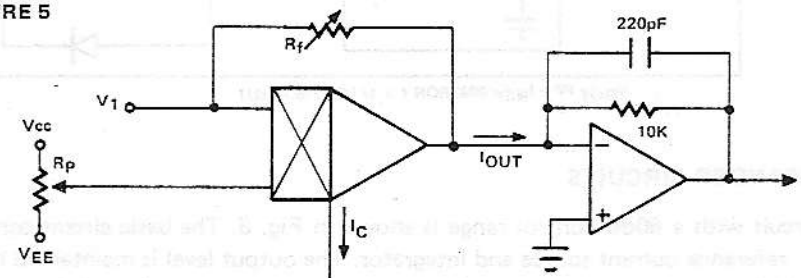


FIGURE 5a

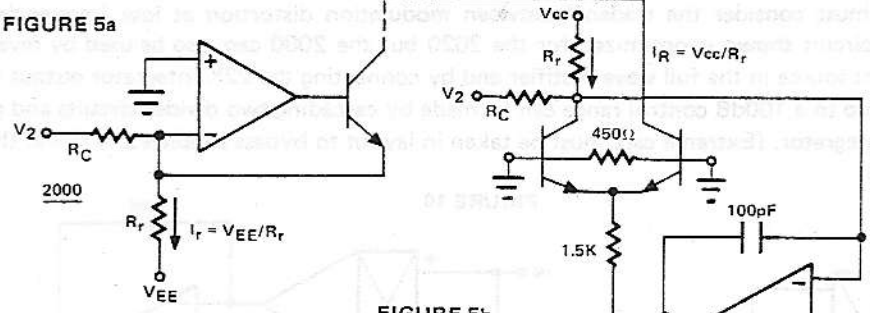
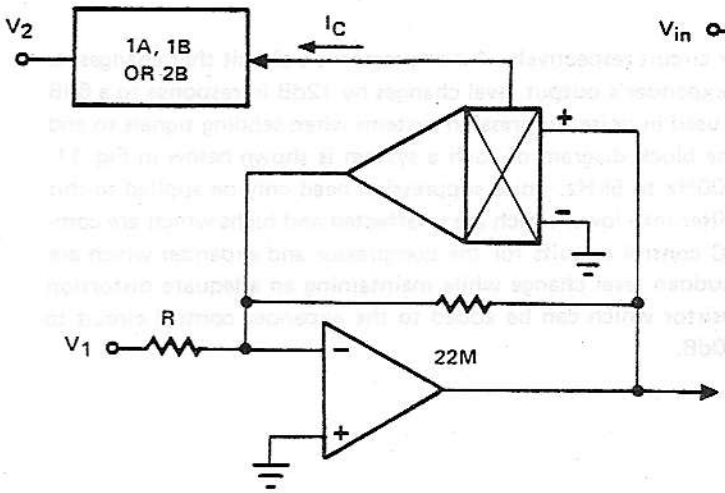


FIGURE 5b

FIGURE 6



V_e = 11.8V, 2000
V_e = 14V, 2020

FIGURE 7

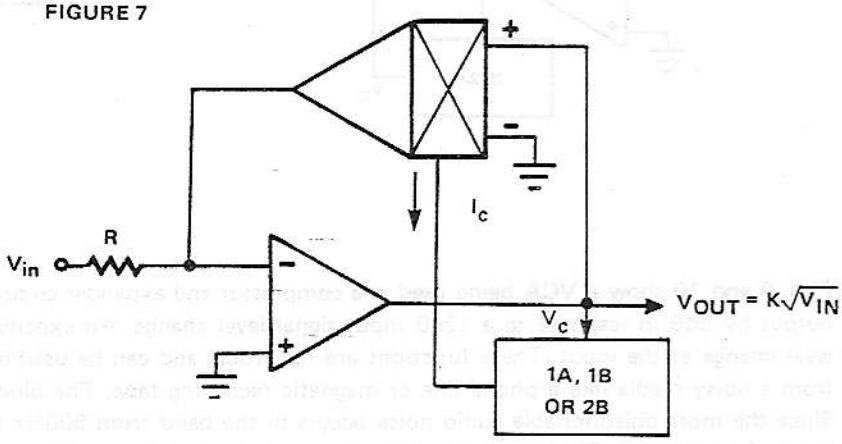
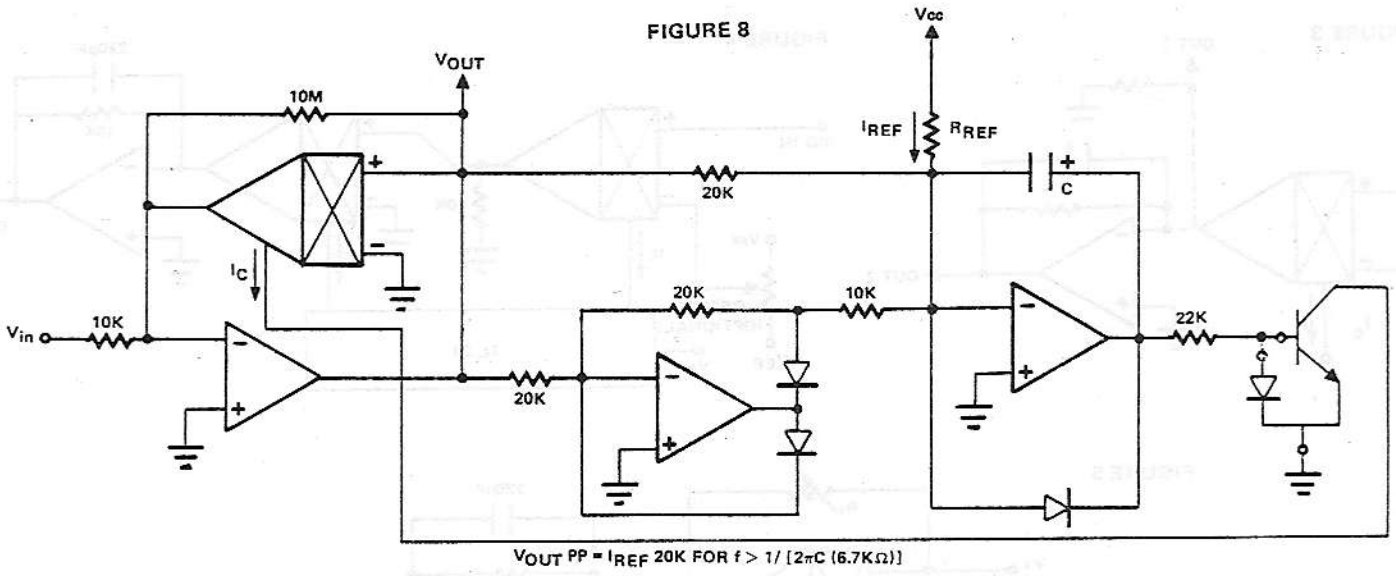


FIGURE 8



$V_{OUT\ PP} = I_{REF}\ 20K$ FOR $f > 1/[2\pi C\ (6.7K\Omega)]$

AGC, COMPRESSOR, AND EXPANDER CIRCUITS

An Automatic Gain Control Circuit with a 60dB control range is shown in Fig. 8. The basic circuit consists of a divider shown in Fig. 6 plus a full wave rectifier, reference current source and integrator. The output level is maintained by forcing the average output of the full wave rectifier which is connected to the signal output to be the same as the reference current. In choosing the C value for the integrator one must consider the tradeoff between modulation distortion at low frequencies and response time to change of input level. The circuit shown is optimized for the 2020 but the 2000 can also be used by reversing the direction of the diodes and reference current source in the full wave rectifier and by connecting the 22K integrator output resistor to the Con In pin of the 2000. An AGC with up to a 100dB control range can be made by cascading two divider circuits and ganging the two VCA sections to the output of the integrator. (Extreme care must be taken in layout to bypass supplies and shield the summing modes of the dividers from stray signals.)

FIGURE 9

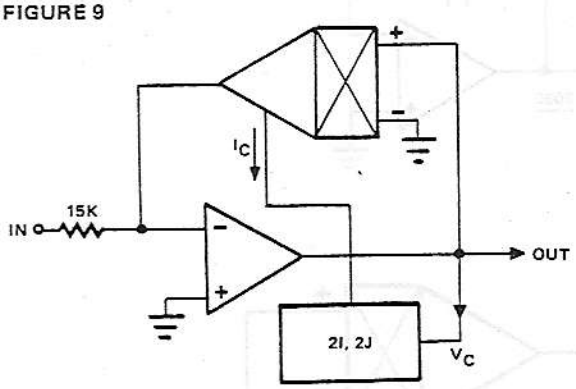
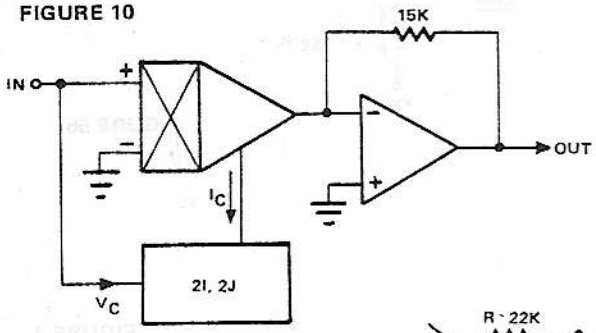


FIGURE 10



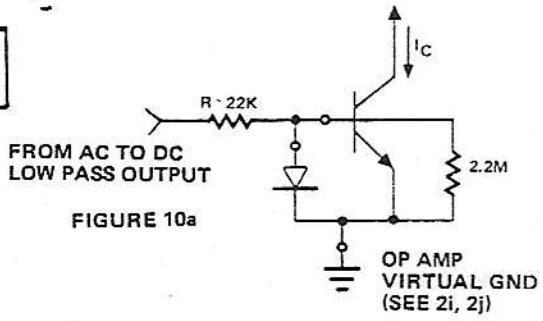
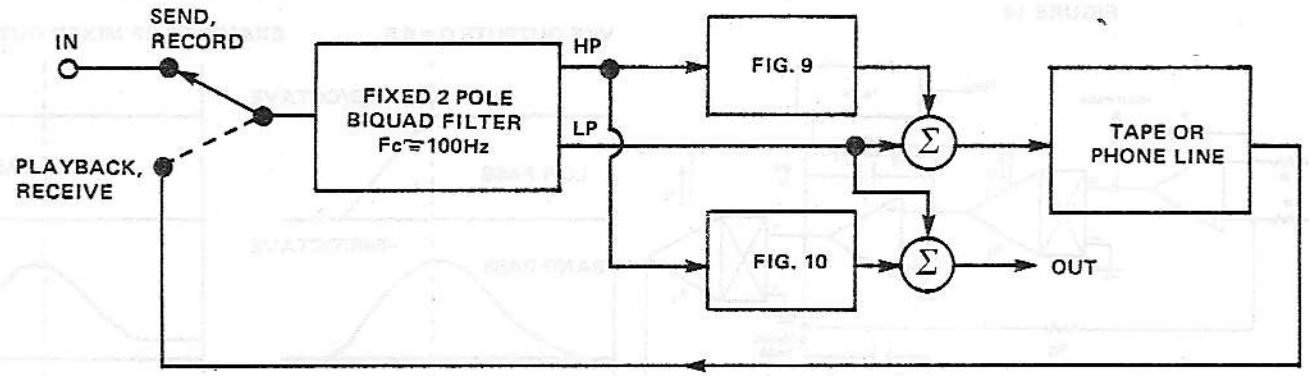


FIGURE 10a

Figs. 9 and 10 show a VCA being used in a compressor and expander circuit respectively. A compressor is a circuit that changes its output by 6dB in response to a 12dB input signal level change. An expander's output level changes by 12dB in response to a 6dB level change at the input. These functions are reciprocal and can be used in noise suppression systems when sending signals to and from a noisy media like a phone line or magnetic recording tape. The block diagram of such a system is shown below in Fig. 11. Since the most objectionable audio noise occurs in the band from 500Hz to 5kHz, noise suppression need only be applied to this band of frequencies. The signal to or from the media is divided by a filter into lows, which are unaffected and highs which are companded. This enables one to choose filter capacitors in the AC to DC control circuits for the compressor and expander which are small enough to give good dynamic performance in response to a sudden level change while maintaining an adequate distortion figure for all audio signal components. Figure 10a shows a 2.2M resistor which can be added to the expander control circuit to produce a noise gate for the highs when the signal level falls below -60dB.

FIGURE 11



MIXERS, FADERS AND PANNING CIRCUITS

Fig. 12 is the basic circuit for voltage controlled mixing. This circuit can be expanded to accomodate more inputs by connecting additional VCA outputs to the summing mode of the op amp. Two Fig. 2b control circuits can be used to independently control the mix level from the two inputs. If control is ganged by using circuits 2g or 2h, a voltage controlled pan or center-off mix can be implemented.

Stereo panning can be accomplished by using two Fig 12 circuits and controlling one with the inverted control signals of the other. This will produce an effect where the right and left sound sources will change sides with an equal monoral mix in the center. With two more Fig. 12 circuits this concept can be extended to quadraphonic systems for interesting spacial and rotating sound effects.

Fig 13 is a control circuit for an automated mixer-fader using Fig 12. With the digital input high, only the A input appears at the output under exponential control of V. When the logic input goes low the A level decays to zero and the B level attacks to a level controlled by V_2 with a time constant ½ RC. The transition between the two sound sources is smooth and pleasant to the ear.

FIGURE 12

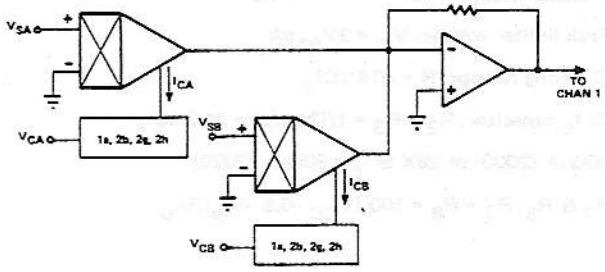
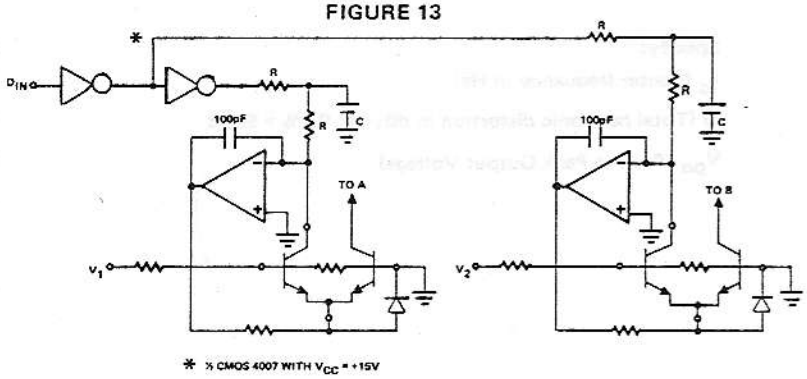


FIGURE 13



VOLTAGE CONTROLLED FILTERS AND EQUALIZERS

Using the circuit in Fig. 14 a voltage controlled filter with a 10,000 to 1 control range or more can be implemented. The low and high pass outputs have 12dB/octave rolloffs and the band pass output has 6dB/octave skirts. Such circuits can be seried to produce more complex filters. In this application a dual VCA can be thought of as a pair of matched voltage controlled resistors. The R_a in the design equation for the cutoff frequency given next to the figure is 21.2K for the 2000 and 28K for the 2020 when the control current in both halves of the device is 500 μA. At 50 μA control current, the value of the R_a will increase by a factor of 10 and so forth. For control ranges of 1000 to 1 or greater, low input bias op amps should be used in the control circuit and signal section of the filter. The LF356 and the TL084 quad op amp perform well offering low input bias, low noise and wide power bandwidth. If antilog control is used, the greatest control accuracy for a 10,000 to 1 range is obtained for control currents of 500 μA to 50 nA. VCA's used in an output mixer with fixed or voltage controlled filters can implement a remote-controlled or automated equalizer. Fig 15 is a VCF that has, in addition to cutoff frequency control, a Q that can be voltage controlled from less than 0.5 to 250. This filter has the additional feature that the gain remains constant at max pass. Low input bias wide band-width op-amps must be used in this circuit to achieve the stated performance over the entire audio frequency range.

For other filters that can be used with the 2000 and 2020 see "Active Filter Cookbook", Don Lancaster; Howard W. Sams and Co.

FIGURE 14

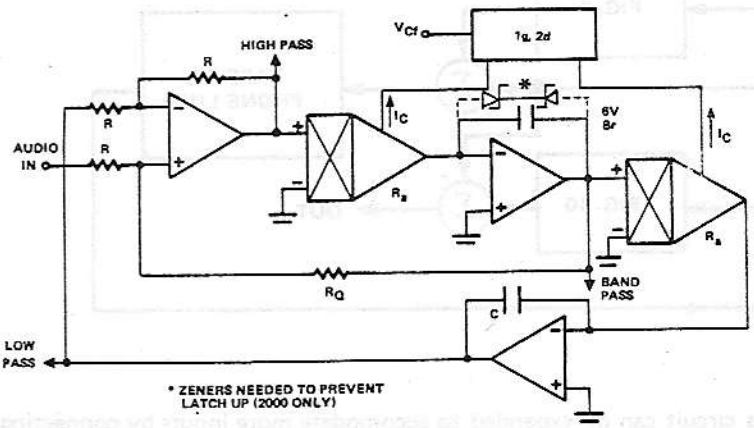
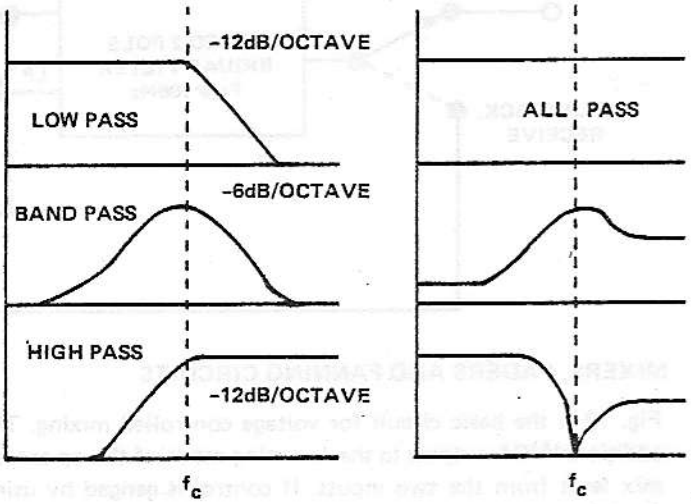


TABLE 2. VCF OUTPUTS & MIXED OUTPUTS



DESIGN EQUATIONS

$R = 10K$ $R_a = 28K @ 500\mu A$ (2020)

$R_a C\omega_o = 1$ $A = 2 - 1/Q$

$R_a = 21.2K @ 500\mu A$ (2000) $R_Q = (2Q-1)R$

VOLTAGE CONTROLLED QUADRATURE OSCILLATOR

The wide range voltage controlled oscillator circuit shown in Fig.16 is very similar to the voltage controlled filter. An extremely low distortion sine wave (approximately 0.1%) can be produced using this circuit. As in the filter, the dual VCA is used as a pair of voltage controlled resistors to tune a biquad stage. All the design tips given for the VCF also apply here. The design procedure is:

Specify:

f_o (Center frequency in Hz)

D (Total harmonic distortion in dB. i.e., 0.1% = 60dB

V_{po} (Peak to Peak Output Voltage)

Find:

1. Transfer ratio; $r = 10^{((D-9)/20)} = 8Q$
2. Peak limiter voltage; $V_{lp} = 2V_{po}\pi/r$
3. Q setting resistor; $R = r/16\pi Cf_o$
4. C: f_o capacitor; $R_2 = R_3 = 1/(2\pi Cf_o) = 21.2K @ I_c =$ $500\mu A$ (2000) or $28K @ I_c = 500\mu A$ (2020)
5. R_7 & R_8; $R_7 = R_8 = 100\ (V_{CC} - 0.6 - V_{lp})/V_{lp}$

NOISE, DISTORTION, OFFSET, AND CONTROL REJECTION

The output signal to noise ratio of the 2000 into a 10K metal film resistor with an input signal of 10 volts peak to peak is 80dB almost independent of the control current in the high end of the control range. The total harmonic distortion is linearly dependent on the input signal amplitude. Typical values are 0.7% with a 10 volt peak to peak signal and 0.07% with a 1 volt signal, etc.* The signal to noise of the 2020 under the same conditions as the 2000 is about 84dB and THD is typically less than 0.1% for all input levels less than 6 Vpp.

Offset in the 2000 and 2020 is best thought of referred to the output rather than the signal inputs. Due to the nature of the design, the D.C. offset appearing at the output will be a small fraction of the control current; typically, 2% with both signal inputs grounded. If the control current is kept under $500\mu A$, the offset can be trimmed out by a pot stretched between the supplies and with the wiper connected to one of the signal inputs.

Offset and control rejection are related and both can be trimmed out with the same adjustment. Control rejection for the 2000 is typically 20dB untrimmed and 46dB trimmed. The corresponding figures for the 2020 are 24dB and 56dB respectively.

*Note: If the circuits in figures C or G are used as control circuits to gang both sides of the SSM2000 to the same control voltage, the distortion figure is doubled and includes some second harmonic distortion. Using two control circuits with a common input with avoid this.

FIGURE 15

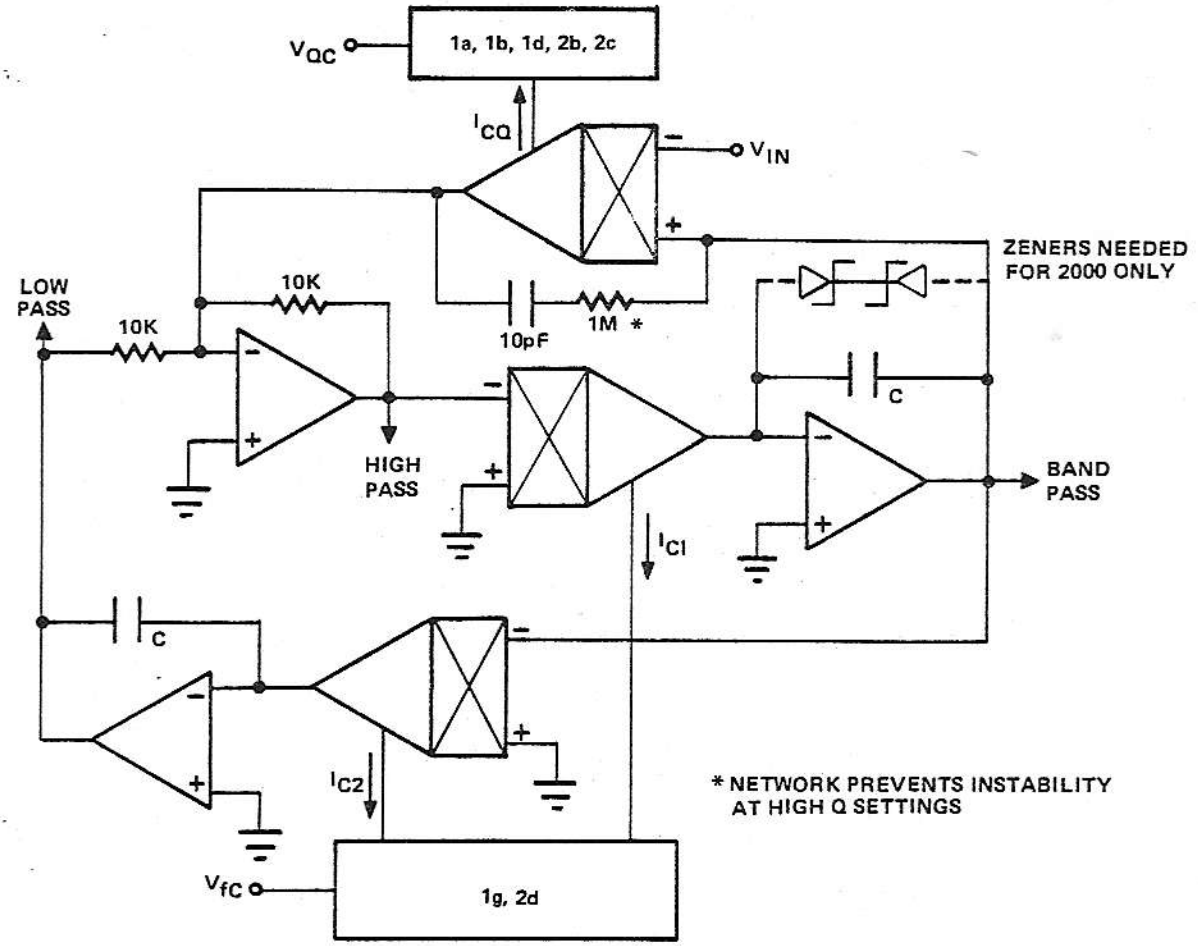


FIGURE 16